EDN
VOICE OF THE ENGINEER
SEPT. 22
Issue 18/2011
www.edn.com


Join the Adventure!
Follow
Learn
Win
FOLLOW daily blogs, video updates, and broadcasts from EE Life editor and road warrior Brian Fuller
LEARN about supply chain options, industry icons and innovators along the way
WIN weekly prizes and earn points to become eligible to win an electric car of your own
START your engines!
DRIVEFORINNOVATION.
driveforinnovation.com
TE
connectivity
Authorized Distributor

EDN®

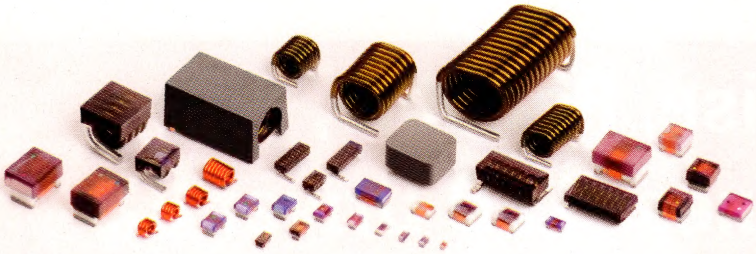
VOICE OF THE ENGINEER

SEPT 22
Issue 18/2011
www.edn.com

MODERN SENSORS GREATLY ENHANCE CONSUMER-ELECTRONIC-SYSTEM PERFORMANCE

Page 38

Why Coilcraft <u>wirewound</u> chip inductors are your #1 choice



Higher Q Compared to non-wirewounds, our chip inductors usually have Qs that are 50 to 150% higher.

Lower DCR Put up to 3 times more current through our chip inductors thanks to their low DC resistance.

Higher SRF The solenoid winding of our inductors gives them a much higher SRF than multilayer parts.

Tighter tolerance Precision manufacturing lets us consistently make parts with ±2% inductance tolerance. Many popular values also come in ±1%.

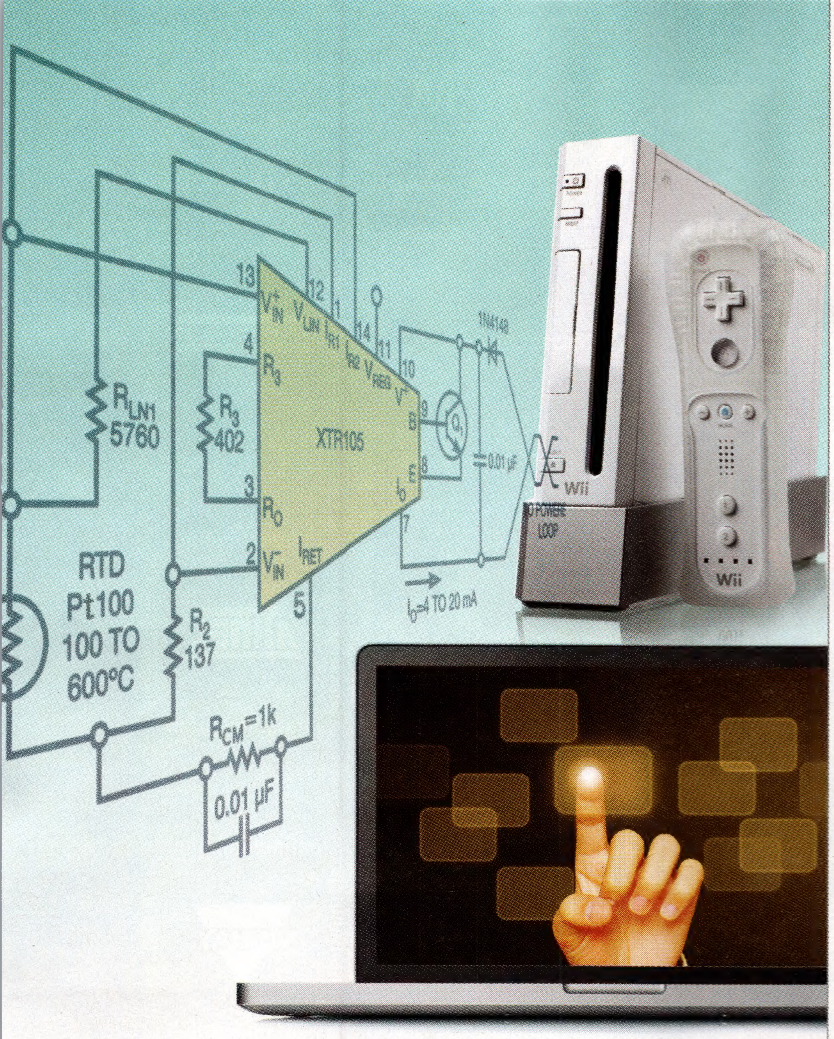
Better support With our engineer-friendly web site, interactive design tools and generous free samples, Coilcraft is just plain easier to do business with.

Visit **www.coilcraft.com** for information on all our high performance wirewound inductors.

coilcraftdirect.com
No min order. Next day delivery.

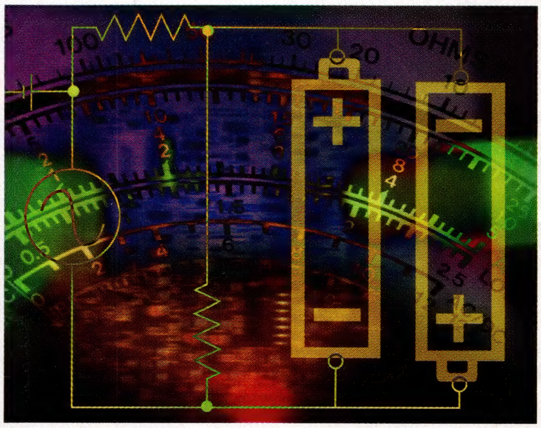
Coilcraft®

WWW.COILCRAFT.COM



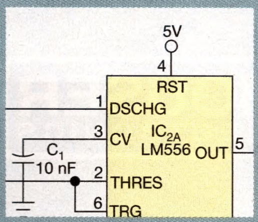
EDN contents

9.22.11



COVER: DAVID NICASTRO/IMAGES: ISTOCKPHOTO.COM

DESIGNIDEAS



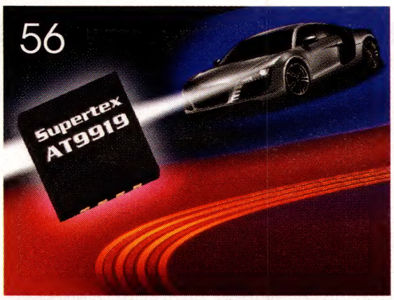
▶ Find out how to submit your own Design Idea: http://bit.ly/DesignIdeasGuide.

mouser.com
Semiconductors and electronic components for design engineers.
Authorized Distributor
Texas Instruments
MAXIM
INNOVATION DELIVERED
Microchip
FAIRCHILD
SEMICONDUCTOR
infineon
It's hip to be square.
freescale
semiconductor
ATMEL
ON
ON Semiconductor
Lattice
Semiconductor Corporation
ST
VISHAY
NXP
FTDI Chip
SILICON LABS
CYPRESS
PERFORM
Advanced semiconductor solutions to fuel your creativity.
Come to Mouser first for what's next from these industry leaders.
mouser.com
The Newest Products For Your Newest Designs
MOUSER ELECTRONICS
a tti company
A BERKSHIRE HATHAWAY COMPANY
Mouser and Mouser Electronics are registered trademarks of Mouser Electronics, Inc. Other products, logos, and company names mentioned herein, may be trademarks of their respective owners.

contents 9.22.11

pulse

DEPARTMENTS & COLUMNS



58

EDN® (ISSN# 0012-7515) is published semimonthly by UBM Electronics, 600 Community Drive, Manhasset, NY 11030-3825. Periodicals postage paid at Manhasset, NY, and at additional mailing offices. SUBSCRIPTIONS—Free to qualified subscribers as defined on the subscription card. Rates for nonqualified subscriptions, including all issues: US, $150 one year; $250 two years; $300 three years. Except for special issues where price changes are indicated, single copies are available for $10 US and $15 foreign. For telephone inquiries regarding subscriptions, call 847-559-7597. E-mail: edn@omeda.com. CHANGE OF ADDRESS—Notices should be sent promptly to PO Box 47461, Plymouth, MN 55447. Please provide old mailing label as well as new address. Allow two months for change. NOTICE—Every precaution is taken to ensure accuracy of content; however, the publishers cannot accept responsibility for the correctness of the information supplied or advertised or for any opinion expressed herein. POSTMASTER—Send address changes to EDN, PO Box 47461, Plymouth, MN 55447. CANADA POST: Publications Mail Agreement 40612608. Return undeliverable Canadian addresses to BleuChip International, PO Box 25542, London, ON N6C 6B2.

Volume 56, Number 18 (Printed in USA).

EDN online

JOIN THE CONVERSATION

Comments, thoughts, and opinions shared by *EDN*'s community

In response to Paul Rako's editorial, "Those crazy engineers," at http://bit.ly/nAjjtb, Larry Sears commented:

"This is exactly why many of us, without regard for obvious insanity, will spend hours and days repairing some ancient, worthless piece of test equipment—just so we end up with an ancient, worthless piece of working test equipment."

In response to "Watch out for well-made (counterfeit) chips," posted in Margery Conner's PowerSource blog at http://bit.ly/ndRSFv, Vin R commented:

"Counterfeit parts are a huge liability for any company that develops critical electronics systems. ... To suggest that parts perform better after thermal soak is not the same as putting them in a solder pot to remove them or removing them from a circuit card over a coal fire. I personally would not want to support recycled parts the way it currently stands from the humanitarian standpoint. ... Destroying people's health in other countries so we can buy cheap products is not OK."

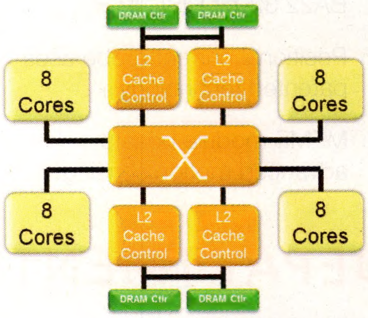
In response to "Are you violating your op amp's input-common-mode range?" written by Todd Toporski, Texas Instruments, at http://bit.ly/oJ10Q5, Stephen R Fleeman commented:

"I tell my students that each input pin of the op amp must remain within the common-mode input range roughly bounded by the supplies. As a young engineer, I tried to use op amps in power-up reset circuits. This is particularly difficult as the supplies are climbing. After hurting my ego and my supervisor's expectations, I told myself that well-behaved discrete devices are much more predictable in those applications."

EDN *invites all of its readers to constructively and creatively comment on our content. You'll find the opportunity to do so at the bottom of each article and blog post. To review current comment threads on EDN.com, visit this page: http://bit.ly/EDN_Talkback.*

CONTENT

Can't-miss content on EDN.com



THE PUZZLE OF MANY CORES

While the PC and server markets gradually evolve from four to six or eight massive x86 cores, Hot Chips papers suggest that the rest of the world is moving in a different direction: large numbers of relatively simple CPUs. As the number of cores grows, how do you deal scalably with interconnect, memory hierarchy, coherency, and intra-thread synchronization?

http://bit.ly/pmTh8f

3-D ICs WITHOUT TSVs?

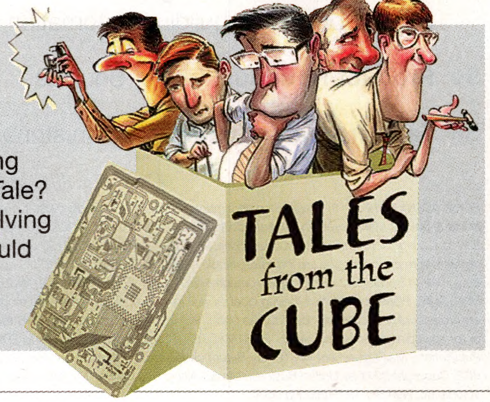
The future of Moore's Law may lie with 3-D ICs. But do 3-D ICs have to use through-silicon vias? One new venture says no.

http://bit.ly/qOX0bQ

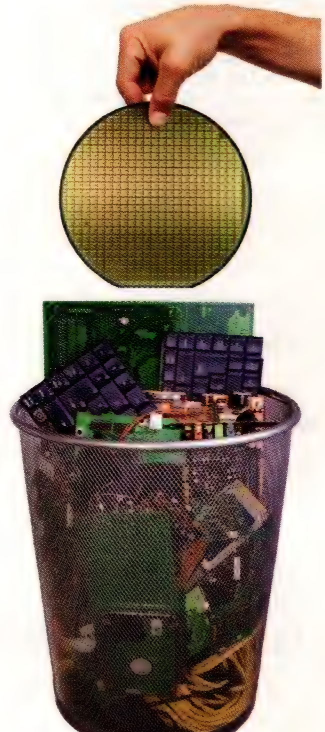
ENGINEERING COMMUNITY

Opportunities to get involved and show your smarts

In *EDN*'s Tales From The Cube, engineers relate their most vexing design challenges—and how they conquered them. What's your Tale? Tell us about a memorable experience you've had successfully solving an engineering problem at work or in your spare time, and you could win a Tektronix scope! **Visit this page for contest information: http://bit.ly/Tales_EDN.**



BY PATRICK MANNION, DIRECTOR OF CONTENT



Silicon's not irrelevant after all!

My experience with the ViewSonic gTablet and its fascinating, hackerlike Android ecosystem, combined with Google's recent purchase of Motorola Mobility, gets me thinking that maybe, just maybe, silicon may still be relevant after all. In 2008, I laid out the premise for silicon's irrelevance on our sister site, *EE Times* (**Reference 1**). I wrote that piece against the backdrop of exponentially rising cost for ASIC development and the increasing performance per milliwatt and per square millimeters and falling costs that continue to make profitable hardware—and ICs—a tough row to hoe.

Some of those overlying trends at the time included the rise of the iPhone and its use of decent hardware and great software; the construction of "solution-to-go" kits from both manufacturers and distributors alike as they strove to add value; and IC manufacturers' concerns about whether their true value lay in the hardware or in the software. It's clear that the industry needs a balance between software and hardware, but hardware guys continue to put more features into smaller form factors at lower cost.

Last year, a product manager at Maxim bragged about how one of the company's analog front ends had greater capability at lower cost and could be applied across multiple high-end devices. Isn't the goal to have highly differentiated ICs for high-end applications to get the margins necessary to research and develop the next iteration?

Meanwhile, software is gathering more headway. Apple's iOS rules, and Android is coming along fast. It's time for hardware to step aside and let software take the spotlight. Given my own hardware background, all this information is a bit jarring.

I got my ViewSonic gTablet a couple of weeks ago so I could play with it before tearing it down for a presentation. At first, I wasn't impressed. The interface seemed sluggish, and the wireless connection was iffy. Worse yet, ViewSonic had walled off the much-hyped Android market, instead confining me to Handango. I pursued it online and found out that a hackerlike phenomenon, ROM rooting, can turn a shabby little knock-off device into the next big thing. Rooting the ROM enables you to give administrative permission to third-party applications to work properly or to their fullest, and it allows applications that need access to system files and specific hardware to function properly.

As a recent blog post (**Reference 2**) points out, you can turn the gTablet's solid, underlying hardware into "the best performing tablet on the market." That hardware includes a 1-GHz Nvidia Tegra 2 with 512 Mbytes of RAM; 16 Gbytes of memory; a 10.1-in. screen with 1080p playback and 1024×600-pixel resolution; a 3650-mAhr lithium-ion battery; a 1.3M-pixel, front-facing camera; and an 802.11g/n wireless connection—all in Android Version 2.2.

By the way, you can access plenty of coursework on Android at the upcoming ESC (Embedded Systems Conference) Boston next week. Start by taking the Fundamentals of Android course in advance and get your certificate at ESC after attending the Android workshop (**references 3** and **4**).

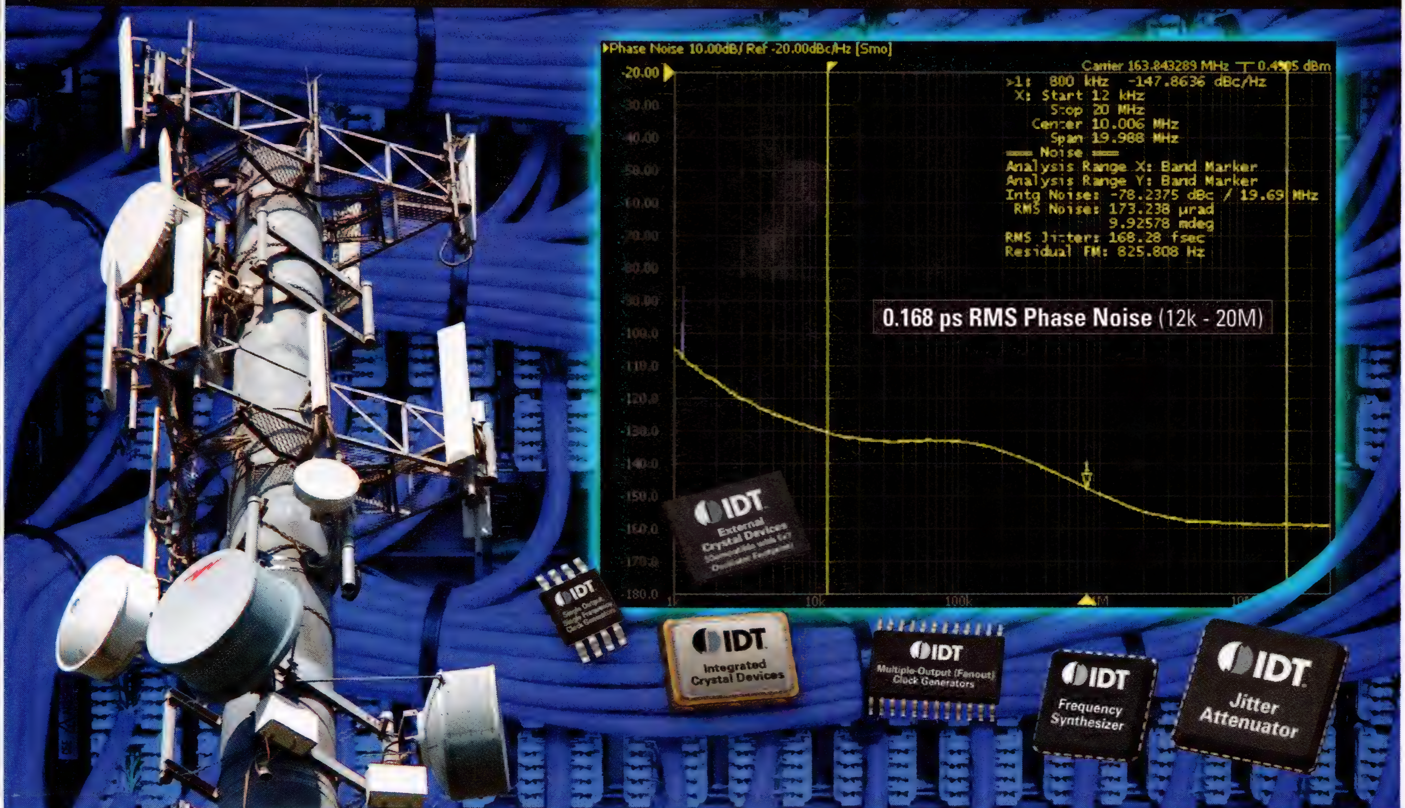
These events again make me think of Google's recent acquisition of Motorola Mobility. After years of flying high as a "we-don't-care-about-no-stinkin'-hardware" software company, Google realized that all the intellectual property that went into developing those handsets, systems, and devices is important after all and that it had better put a stake in the ground. **EDN**

REFERENCES

1. Mannion, Patrick, "Opinion: the irrelevance of silicon," *EE Times*, April 25, 2008, http://bit.ly/oruXOM.
2. Cooter, Josh, "How To: Unleash The Power Of The Viewsonic G Tablet And Turn It Into The Best Performing Tablet On The Market," *Android Police*, http://bit.ly/o0SNYu.
3. "Fundamentals of Google Android," *EE Times*, March 2010, http://bit.ly/pT3tL7.
4. "Android Certificate Program," Embedded Systems Conference, September 2011, http://bit.ly/nLgeLC.

Contact me at patrick.mannion@ubm.com.

Integrated Device Technology FemtoClock NG – When a Trillionth Of a Second is Just Too Long



The FemtoClock Next Generation (NG) clock synthesiser family allows engineers to generate almost any output frequency from a fixed frequency crystal, and to meet the challenges of the most demanding timing applications.

Use of a single source to generate multiple clocks often leads to increased susceptibility to power supply noise and restrictions on multiplication factors. IDT's technology effectively eliminates these problems by doubling the power-supply noise rejection (PSNR) of previous generation devices while also introducing the potential for virtually limitless customization of output frequency.

An innovative fractional multiplier PLL architecture introduces the flexibility for engineers to generate any output frequency from any input frequency. And the advanced design of the FemtoClock NG family achieves greater than 80 dB of PSNR to make the devices immune to power-supply noise.

Other performance benefits of FemtoClock NG technology include low power consumption and a clocking performance of under 0.5 ps RMS phase noise jitter! The devices offer standard outputs such as differential LVPECL, LVDS and single-ended LVCMOS, providing a precise fit to any application.

With FemtoClock NG technology, IDT has eliminated the most challenging aspects of silicon-based clock design and introduced an unprecedented level of flexibility for clocking in high-performance applications.

IDT®
Integrated Device Technology

The Analog and Digital Company™

For more information visit us online at www.IDT.com

EDITED BY FRAN GRANVILLE

pulse

INNOVATIONS & INNOVATORS

Mains-current-data logger monitors one- and three-phase ac systems

The PicoLog CM3 USB (Universal Serial Bus)/Ethernet current-data logger measures the power consumption of buildings and machinery. With three channels, it can monitor current in single- and three-phase ac installations. Applications include monitoring three-phase motors and generators, measuring the consumption of HVAC (heating/ventilation/air-conditioning) systems, and balancing phases in multiphase supplies. The logger comes with three ac current clamps and a data-acquisition-software package.

The PicoLog CM3's measuring range is 0 to 200A, with an accuracy of ±1% and less than 10 mA of noise. Conversion resolution is 24 bits. The current clamps comply with IEC1010-1 (1995) and with EN61010-1 (2001) Category II 600V and Category III 300V.

The data-logging software runs on any PC with Windows XP or later versions. PicoLog can collect data from as many as 20 PicoLog CM3s at programmable intervals from 720 msec/channel to minutes, hours, or even days. It displays readings in a monitor window with optional limit alarms, alongside optional live graph and table views of the same data. You can export readings in a standard text format compatible with other spreadsheet and analysis programs.

A software-development kit is also included. The kit contains Windows DLLs (dynamic-link libraries), drivers, and code, allowing you to integrate the device into your own software. The dual USB/Ethernet interface lets you place the data logger anywhere from your desktop to the other side of the world. The CM3 can operate as a USB-only device, as a USB-powered device with an Ethernet interface, or as a POE (power-over-Ethernet) device.

The PicoLog CM3 sells for £349 (approximately $575) and comes with free technical support and a free five-year parts-and-labor warranty against manufacturing faults.

—by Colin Holland

▷**Pico Technology**, www.picotech.com.

Applications for the PicoLog current-data logger include monitoring three-phase motors and generators, measuring the consumption of HVAC systems, and balancing phases in multiphase supplies.

TALKBACK

"Last time I persevered through an intractable technical problem and then presented the solution, I had to run to the towel dispenser for all the vapid drooling. Yes, fix those technical problems, but do it quickly and discreetly." —Analog engineer "Ypresian," in *EDN's* Talkback section, at http://bit.ly/nmdvY4. Add your comments.

Cast announces royalty-free BA22 32-bit RISC IP

Some designs need a CPU core but not an ARM core. The issue may simply be avoiding royalties, avoiding export restrictions, or complying with a corporate policy. Alternatively, it may be that you are trying to hit a speed-area-power point that is a stretch for ARM's (www.arm.com) current products and you don't want to invest in an expert in processor-core optimization. This situation can easily come up when a legacy design using an 8- or 16-bit core runs out of steam, for example, and needs to migrate to 32 bits.

One option would be to use an open-source CPU core, such as the open-SPARC S1, the Leon, or the more specialized Lattice Semiconductor (www.latticesemi.com) LatticeMico 32. With such open-source cores, however, you may be on your own for verification and integration. Another alternative would be a commercial core, such as one employing the BA2 architecture from Slovenian IP (intellectual-property) vendor Beyond Semiconductor (www.beyondsemi.com). This choice recently became more attractive with the announcement that three preconfigured versions of Beyond's BA22 core are now available under royalty-free license from IP supplier Cast.

The BA22 family, according to Nikos Zervas, Cast's vice president of marketing, is what you'd get if you started out with a clean sheet of paper, without constraints from a decades-old instruction-set architecture and with the latest thinking in compact, low-power design. In this scenario, you would have few enough constraints to produce some impressive results, and it appears that Beyond has done so. According to Zervas, a study from technology-analysis and -consulting company Linley Group (www.linleygroup.com) finds the BA22 instruction stream 5 to 20% denser than ARM's Thumb-2. The company goes on to claim implementations as small as 12,000 gates, operating dynamic-power consumption of as little as 23 μW/MHz in a—presumably low-power—65-nm process, and 1.4 DMIPS/MHz, all from a fully synthesizable core.

The preconfigured cores are the BA22-Base, the BA22-Adv (advanced), and the BA22-AP (application processor). The BA22-Base is the compact member of the family. It synthesizes to fewer than 15,000 gates and can reach 350 MHz at 65 nm. The configuration includes either an AMBA/AHB (Advanced Microcontroller Bus Architecture/Advanced High-Performance Bus) or a Wishbone bus controller, dedicated ports for on-chip instruction and data memories, and an integral interrupt controller and power-management engine. The engine manages power modes through a combination of dynamic clock gating at the unit level and software-controlled clock-throttling—nothing that should present huge integration challenges. An optional debugging engine is also available. According to Zervas, this configuration gives deeply embedded controller applications—especially those moving from 8- or 16-bit architectures—easy access to 32-bit tools and performance.

The BA22-Adv is essentially the same Base core with the addition of 16 general registers—for a total of 32—and instruction and data caches. It targets larger systems that require off-chip memory—hence, the caches—and those that will run an RTOS. Cast puts the core at about 19,000 gates, with operation as fast as 300 MHz at 65 nm. Ports of the eCOS (embedded configurable operating system) and uClinux RTOS kernels are available.

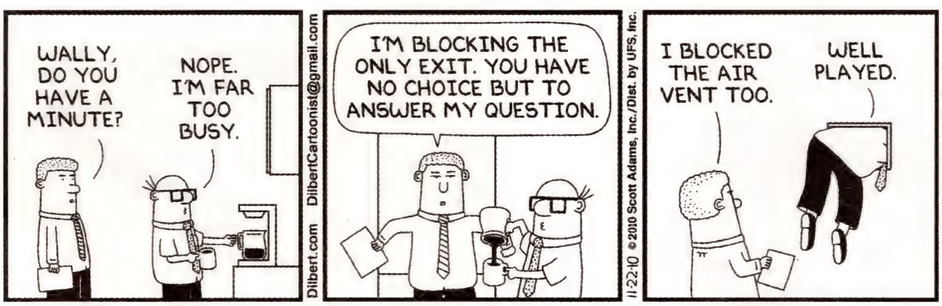
The BA22-AP adds instruction and data MMUs (memory-management units) to the Adv configuration. The AP also offers the option of floating-point, divider, and multiply/accumulate units. The core synthesizes to 35,000 gates in a 90-nm process, the company claims, although it's not clear what that number includes. I suspect that it does not include the added arithmetic units, the TLBs (translation-look-aside buffers), or the caches. In the 65-nm benchmark process, the core hits 300 MHz, the company claims. The AP is an application processor rather than a deeply embedded controller. Accordingly, Zervas says, ports of Linux and Android are available. He claims that the core has application throughput similar to that of a Cortex R4.

> “The BA22 may lack the processor-validation programs of the ARM cores, but it is silicon-proven at major houses.

All the BA22 cores come with a gcc-based Eclipse environment. Cast offers a variety of optional modules for the cores and a range of compatible peripheral and accelerator cores. The company can provide preconfigured subsystems and integration support. Although the BA22 may lack the exhaustive processor-validation programs of, say, the ARM cores, it is silicon-proven at major houses, such as OmniVision (www.ovt.com) and STMicroelectronics (www.st.com). The three BA22 cores are available now, as is the development environment for Linux. A Windows port of the environment should become available this fall. **—by Ron Wilson**

▷**Cast**, www.cast-inc.com.

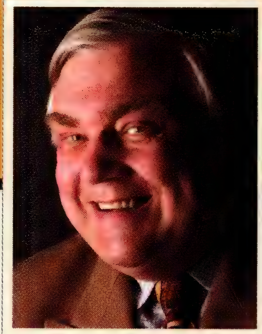
DILBERT By Scott Adams



RAQ's

Rarely Asked Questions

Strange stories from the call logs of Analog Devices



Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur. Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

The Benefits of Ancient Logic

Q. What sort of logic circuitry should I use in (mostly) analog circuitry?

A. Ancient logic! Not microprocessors, or fast modern logic types, but old slow 4000 Series CMOS. It's not quite as old as Stonehenge[1] but the 4000 Series contains many valued ancient monoliths.

Analog circuitry often needs a little logic, or perhaps a simple oscillator or timer, but it may not operate from logic supplies, and fast logic generates switching noise.

4000 Series CMOS, still widely available[2] despite its age (>40 years), is ideally suited for this application. Working with supplies from 3 V to 15 V (sometimes 18 V), its current consumption is low; it does not draw brief, but large, pulses of current when switching; and because it is slow it is quiet.

Some 4000 Series devices (4093 quad NAND gate and 40106 hex inverter, for example) have Schmitt trigger inputs and can create square waveforms from slow analog inputs with few additional components. These devices may also be used in simple oscillators, timers, and pulse generators.

Because the input current of 4000 Series devices is low, and we are not usually worried about speed in these applications, the logic may be made more complex, where necessary, by adding diode/resistor AND or OR logic at the inputs. The 5 pF to 7 pF input capacitance may be used, in conjunction with high value series input resistors, to generate time delays of several microseconds.

The 4000 Series includes the 4046 phase-locked-loop (PLL) circuit, which has a useful phase comparator and a convenient, though low performance, voltage-controlled oscillator (VCO)[3]. Many other useful small- and medium-scale logic functions are available in the family.[4]

There are, of course, disadvantages: timers and oscillators made with the 4000 Series have poor temperature and supply voltage sensitivity, and the oscillators have poor phase noise; complex logic, unless it happens to be available as an MSI function, will require several devices to fabricate it; and the devices are available only in DIL and SOIC packages.

Nevertheless, the 4000 Series is ideally suited to providing logic and timing functions in predominantly analog circuitry. Offering low switching noise and low power consumption over a wide supply-voltage range, it should always be considered when such functions are needed.

[1] Over 4000 years old, Stonehenge has a slight advantage over the 40-year-old 4000 Series.

[2] The 4000 Series is widely available, but not from Analog Devices.

[3] If a better VCO is required, the AD654 works well with the 4046 phase comparator, and will operate with 5-V to 36-V supplies.

[4] http://en.wikipedia.org/wiki/List_of_4000_series_integrated_circuits

To Learn More About Ancient Logic
http://dn.hotims.com/34942-100

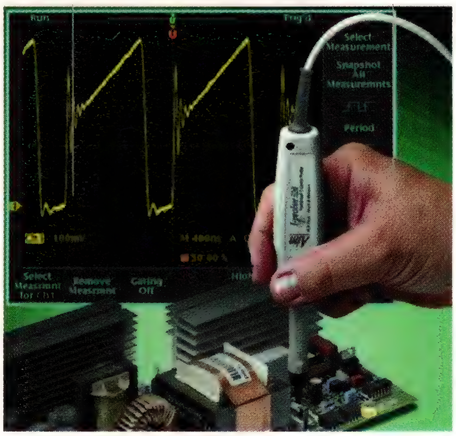
Have a question involving a perplexing or unusual analog problem? Submit your question to: www.analog.com/askjames

For Analog Devices' Technical Support, Call 800-AnalogD

SPONSORED BY ANALOG DEVICES

Positional current probe uses patented technology

Aim-TTi (Aim Instruments/Thurlby Thandar Instruments) has launched a new type of current probe that can measure currents in PCB (printed-circuit-board) tracks. The Aim I-prober 520 positional current probe uses a patented technology to observe and measure current without breaking or surrounding the conductor. Measurement of current normally requires either inserting a shunt resistor or passing the conductor through a closed magnetic loop. This measurement technique typically uses some form of split-clamp device. Whereas this approach is suitable for individual wires, it is of no use for measuring current in PCB tracks. You use the compact, handheld I-prober 520 with an oscilloscope. Placing the insulated tip of the probe onto a PCB track enables you to observe and measure the current flowing in the track.



The Aim I-prober 520 positional current probe uses a patented technology to observe and measure current without breaking or surrounding the conductor.

The probe has a bandwidth of dc to 5 MHz and a dynamic range of 10 mA to 20A p-p. It has a safety rating of 300V for Category II and 600V for Category I and is suitable for connection to any oscilloscope. It operates by sensing the field in close proximity to the track. To achieve a calibrated measurement, the field sensor must be able to maintain a precise distance from the track. To achieve adequate sensitivity, this distance must be short because the field reduces with the square of distance to a first-order approximation. Creating a practical current-measurement probe requires a miniature sensor with precision dimensions, dc-sensing capability, wide ac bandwidth, and low noise. The I-prober 520 uses a patented miniature version of a flux-gate magnetometer, which the company developed with Cambridge University. The technology enables it to measure the field at a precise point in space. The miniature sensor also has much lower noise and much wider bandwidth than a conventional flux-gate magnetometer.

You can also use the probe on component leads or any other current-carrying conductor. An interesting example occurs in ground planes, for which you can use it to observe circulating currents, interference-injection points, and hot spots. The Aim I-prober 520 comes with a control box and a calibrator; a power supply; and a clip-on toroid assembly, which can convert it into a conventional closed-magnetic-loop current probe.

—by Colin Holland

▷**Aim-TTi**, www.aim-tti.com.

MEMS module boasts advanced motion sensing

STMicro's new iNEMO (inertial module) integrates three-axis sensing of linear and angular motion in a 4×5×1-mm package—approximately half the size of competitive devices. The three-axis, 6°-of-freedom MEMS (microelectromechanical-system) module enables users of the company's single-function sensors to upgrade their designs, reaping the package-level integration benefits of size reduction and reliability. The LSM330DLC multisensor module combines a user-selectable full-scale acceleration range from 2 to 16g with angular-rate detection of 250 to 2500 dps along the pit, roll, and yaw axes. The module includes power-down and sleep modes and an embedded FIFO (first-in/first-out) memory block for power management. It can operate with any 2.4 to 3.6V supply voltage.

Applications for the device include motion-activated user interfaces in mobile phones, tablets, and other smart consumer devices; dead-reckoning and map-matching in personal navigation devices; and intelligent power saving and free-fall detection in portable electronics. Using micromachining, the LSM330DLC has an analog supply voltage of 2.4 to 3.6V; digital-supply voltage I/Os of 1.8V; three independent acceleration channels; three angular-rate channels; and an SPI (serial-peripheral interface) and I²C serial interface with 16-bit data output. The ROHS (restriction-of-hazardous-substances)-directive-compliant module is available in engineering samples. Price is $3.20 (1000).

—by Ismini Scouras

▶**STMicroelectronics**, www.st.com.

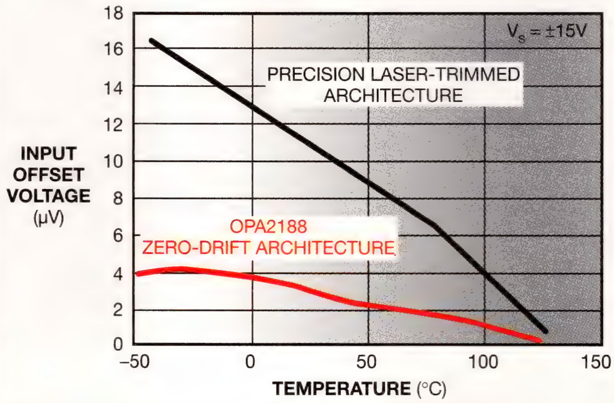
The LSM-330DLC multisensory device integrates three-axis sensing of linear and angular motion in a 4×5×1-mm package.

Ultraprecision op amp pushes to zero drift, 36V rail

Remember that "ideal" op amp from basic-circuits class—the one with no drift, no offset, no errors, and no other issues? IC vendors are continuously getting closer to that ideal: the Texas Instruments OPA2188 dual, ultraprecision op amp has low enough drift that it is in the class the op-amp vendors often refer to as "zero drift." TI achieves this offset-voltage performance through design and process, not laser trim.

The typical and maximum voltage-offset drifts of 0.03 and 0.085 μV/°C, respectively—four times better than those of the closest competitor, according to TI—are not the only specifications that distinguish this op amp, however. The company claims that it is the first zero-drift op amp that can operate from a 36V rail or corresponding bipolar rails, making it a good fit for test and measurement, weight scales, flow meters, and medical instrumentation.

If you live in the single-digit-supply-rail world, you may wonder why anyone would want 36V. It's a voltage that suits use in harsh electrical environments that need higher-voltage rails to maintain analog-signal-chain SNR (signal-to-noise ratio). Input-common-mode range extending from the negative rail to within 1.5V of the positive rail saves additional circuitry and enables 5V, single-supply operation.



The Texas Instruments OPA2188 dual, ultraprecision op amp has zero drift and input offset voltage four times better than the nearest competitor, according to the company.

Despite the 36V rating, the quiescent current per amplifier is 475 μA, enabling portable-medical-system applications. Also benefiting instrumentation applications, the op amp sports initial offset voltage of 25 μV and noise of just 8.8 nV/√Hz.

Tools and support include a $5 universal EVM (evaluation module), which simplifies evaluation by allowing you to easily construct many circuits; a reference design and Spice model in TINA-TI 9.1, a Spice-based analog simulation program; and software for analysis, application, and calculation utilities, including Analog Filter Designer, FilterPro, and calculators for decibel, frequency/wavelength, and op-amp gain stage.

The OPA2188 is available in a 3×5-mm MSOP or 5× 6-mm SOIC package and sells for $1.40 (1000).

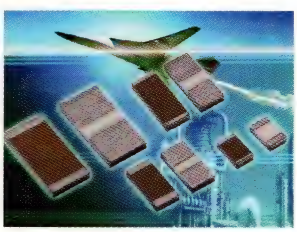
—by Bill Schweber

▷**Texas Instruments**, www.ti.com/opa2188ds-pr.

Chip resistors feature extended-pad design for high-power, high-temperature applications

Vishay's foil-resistor division recently announced a series of ultra-high-precision bulk-metal Z1-foil wraparound, surface-mount chip resistors with extended pads for high-temperature, high-power applications. The new designs target systems operating at temperatures as high as 225°C and offer improved heat dissipation for operating at 1200 and 330 mW at 70 and 200°C, respectively.

Vishay based FRSH on the next-generation Z1-foil technology, whose bulk-metal-foil element's sensitivity to temperature is an order of magnitude lower—both internally and externally—than that of classic foil. It also provides long-term stability in high-temperature environments. FRSH devices offer a TCR (temperature coefficient of resistance) of ±1 ppm/°C from –55 to +125°C and ±2.5 ppm/°C from –55 to +200°C, at a 25°C reference temperature. The resistors feature load-life stability as high as ±0.05% at 200°C for 2000 hours at working power, long-term stability as high as ±0.05% at 225°C for 2000 hours, and tolerances to ±0.02%. The devices' full wraparound terminations ensure safe handling during manufacturing and provide stability during multiple thermal cyclings. The devices can withstand as much as 25-kV ESD (electrostatic discharge) without degradation.



Vishay's FRSH technology uses the next-generation Z1-foil technology, whose bulk-metal-foil element's sensitivity to temperature is an order of magnitude lower—both internally and externally—than that of classic foil.

Available in six chip sizes from 0603 to 2512, the FRSH series features a resistance of 10Ω to 125 kΩ; any resistance value within this range is available at any tolerance with no additional cost or lead-time effect. The resistors feature a rise time of 1 nsec and have effectively no ringing, a thermal stabilization time of less than 1 sec, a current noise of 0.01 μV rms per volt of applied voltage at 40 dB or less, and a voltage coefficient of less than 0.1 ppm/V. The ROHS (restriction-of-hazardous-substances)-directive-compliant devices offer a noninductive, less-than-0.08-μH; noncapacitive design and are available in matched sets. Prices start at $4.73.

—by Ismini Scouras

▷**Vishay**, www.vishaypg.com/foil-resistors.


Name
Dr. Dave Barrett
Job Title
Professor,
Mechanical Engineering
Area of Expertise
Robotics
LabVIEW Helped Me
Bridge the gap between teaching theory and real-world design experience
Latest Project
Building a robotic tuna to swim across the Atlantic Ocean
NI LabVIEW
LabVIEW makes me better by making complex
CONTROL
simple and accessible
>> Find out how LabVIEW can make you better at ni.com/labview/better
800 453 6202

VOICES

Transphorm: GaN-based power devices prove their worth at higher voltages

Early this year, John Palmour, chief technology officer at Cree, discussed with *EDN* the future of high-performance, high-voltage SiC (silicon carbide) in power-switching devices (**Reference 1**). More recently, Carl Blake, vice president of marketing at GaN (gallium-nitride)-based-power start-up Transphorm, discussed his company's February announcement that it is working with selected customers to deliver 600V GaN devices and will have fully qualified devices for sale by year-end. Transphorm's GaN HEMTs (high-electron-mobility transistors) have blocking voltages of 600V and maximum on-resistances of 310 and 180 mΩ, respectively, for the TPH2002PS and TPH2006PS. The following is an excerpt of that interview.

National recently came out with its LM5113 eGaN [enhancement-mode-GaN] FET-driver IC designed especially to ease the challenges of threshold gate voltages on the eGaN devices from EPC [Efficient Power Conversion, Reference 2]. Does Transphorm's process require a similarly tight tolerance on the gate voltage?

A First, some background: GaN transistors are inherently normally on. Power-circuit designers are comfortable working with MOSFETs that perform in a normally off mode, [so] Transphorm has ... combined a normally on GaN HEMT with a low-voltage silicon device connected to the emitter, or source, of the GaN HEMT; it's a cascode connection [the same architecture that International Rectifier plans to use for its next generation of 600V GaN devices].

Nobody has figured out how to make a GaN gate that survives more than 6V. By definition, a normally off device is one that [requires] a positive bias voltage on the gate in order to turn it on, and that positive bias can be as little as 0.5V—at least for the professors in academia, who want to claim that they've made a normally off GaN device. However, in a practical application, 0.5V wouldn't get sufficient noise immunity. You need a higher turn-on voltage.

What EPC did is add a gate section to its GaN device, but in GaN rather than in silicon. The problem with doing it in GaN is that you are still limited to 6V. To get the part fully turned on, you have to apply at least 4.5V to the gate; 1.5V is not much room to control the gate-drive signal over temperature, power-line variations, and variations within the circuit.

The LM5113 was designed specifically to address these challenges. Care to comment?

A There are consequences to trying to hit those tight tolerances. EPC chose one route, and Transphorm chose another.

Transphorm's GaN power transistors and diodes have blocking voltages of 600V and greater. Doesn't that put you head-to-head against power-SiC devices?

A Absolutely, but a 6-in. SiC wafer costs $2500. If you use a SiC substrate, that's your base cost. A 6-in. silicon wafer costs $25, and GaN can be grown on silicon. That's why competition from SiC is not a concern.

But Transphorm also has GaN-on-SiC parts?

A Our initial parts were built on SiC because its crystal structure is a closer match to GaN, and it's a bit easier to build on it. We could get high-voltage parts that were stable [enough to] show to customers [so that they could test them] in circuits.

The parts you've announced you'll introduce at the end of the year—600V, fully qualified—which will they be?

A We're running both qualification programs in parallel. We'll introduce the GaN-on-Si parts and then the GaN-on-SiC parts. ... When we release 600V GaN-on-Si, we'll then start making higher-voltage parts with GaN-on-SiC and basically do the same thing.

You use the SiC platform to bootstrap to the next voltage level, so why aren't you going after the lower-voltage devices?

A The higher the voltage, the more advantage there is to GaN. At 30V, a power converter has to be switching at higher than 1 MHz before there's an advantage to GaN. And, because GaN is a new technology, it's not yet at the cost levels of silicon MOSFETs. So, why would somebody buy a new part that is more expensive if it only matches a silicon MOSFET's performance?

So, on-resistance is not significantly better at less than 200V?

A Right. We looked at the market and asked, Where did the parts add significant value for the customer that *their* customer will get a benefit that is worth paying more for? And that [answer] was easier to find at 600V than at the lower-voltage applications. But solving the problems of higher breakdown voltages was much more difficult.

—interview conducted and edited by Margery Conner

REFERENCES

1 Conner, Margery: "Emerging power technology: silicon carbide," *EDN*, Feb 17, 2011, pg 20, http://bit.ly/qLDmtg.

2 Conner, Margery: "Industry's first eGaN-FET driver simplifies switching design," *EDN*, July 28, 2011, pg 16, http://bit.ly/oIlju1.

BY BONNIE BAKER

Designing with temperature sensors, part one: sensor types

Most people have heard the phrase "Birds of a feather flock together," which describes people who have similar characteristics or interests and choose to spend time together. Is it possible that some temperature sensors tend to flock together, too?

Of the sensing technologies, temperature sensing is the most common due to the multitude of applications in which it is critical to know and process the actual or the relative temperature. For instance, pressure, force, flow, level, and position sensors often require temperature monitoring to ensure accuracy. Most sensors use resistive-bridge configurations to measure pressure and force. The temperature errors of the resistive elements in these bridges can exceed the sensor's actual measurement range, making the pressure sensor's output useless—unless you know the temperature of the bridge. Flow- and level-sensor accuracies depend on the density of the liquid or the gas. The temperature of that material is one variable that affects accuracy.

Today's most popular temperature sensors are thermocouples, RTDs (resistance-temperature detectors), thermistors, and silicon-based sensors. These sensors flock together because these well-characterized devices typically can solve temperature-measurement problems. These sensor technologies cater to specific temperature ranges and environmental conditions. You can use specifications such as the sensor's temperature range, ruggedness, and sensitivity to determine whether the device will satisfy the requirements of the application.

Keep in mind that no one temperature sensor is right for all applications. The thermocouple has an unrivaled temperature range, and the RTD sensor has excellent linearity. **Table 1**, which is available with the Web version of this column at www.edn.com/110922bb, summarizes the main characteristics of thermocouples, RTDs, thermistors, and silicon-based temperature sensors. This **table** can be useful during your first pass in the sensor-selection process.

A thermocouple comprises two wires of dissimilar metals that are bonded together at one end. This configuration produces an EMF (electromotive-force) voltage between the two wires at the unbounded, or measurement, end. The EMF level is a function of the two dissimilar metals and the temperature gradient along the length of the thermocouple wires. The thermocouple is not particularly accurate; however, it can quickly sense over a wide temperature range.

RTDs provide excellent accuracy in a temperature-sensing environment. Their temperature range is narrower than that of thermocouples but wider than those of thermistors and silicon-based sensors. Select an RTD sensor if your application requires a high-quality, accurate temperature measurement.

Thermistors often provide the lowest-cost approach for your temperature-sensing system. You can overcome the devices' high nonlinearity with a simple resistive network. Although this type of network reduces thermistors' temperature range, this trade-off is acceptable in many temperature-sensing applications.

IC-temperature or silicon-based sensors offer another alternative to solving temperature-measurement problems. Their advantages include user-friendly output formats and easy installation during PCB (printed-circuit-board) assembly. Although silicon-based temperature sensors respond slowly due to their package mass, their plug-and-play features make them attractive. **Table 2**, which is also available with the Web version of this column at www.edn.com/110922bb, complements the specifications in **Table 1** with a list of typical applications for these four temperature sensors. Examples of appropriate applications include biophysics and metal-cutting research for thermocouples, cold-junction compensation and calibration for RTDs, pyrometer calibration for thermistors, and battery management for silicon-based sensors.

Of the temperature sensors now on the market, thermocouples, RTDs, thermistors, and silicon-based sensors continue to dominate. The thermocouple is most appropriate for higher-temperature sensing, whereas the RTD is best suited for lower-temperature applications requiring good linearity. The thermistor is a low-cost alternative for applications having smaller temperature ranges, and silicon-based sensors sometimes win out because of their ease of use. The next four Baker's Best columns will dig into the temperature-sensor details of these four families of sensors. EDN

REFERENCES

1 *Product Book*, Thermometrics, 1997.

2 Schraff, Fred, "The Principles and Methods of Using Thermocouples," *Measurement & Control*, June 1996, pg 126.

3 Sulciner, James, "Understanding and Using PRTD Technology, Part 1: History, Principles and Designs," *Sensors*, August 1996.

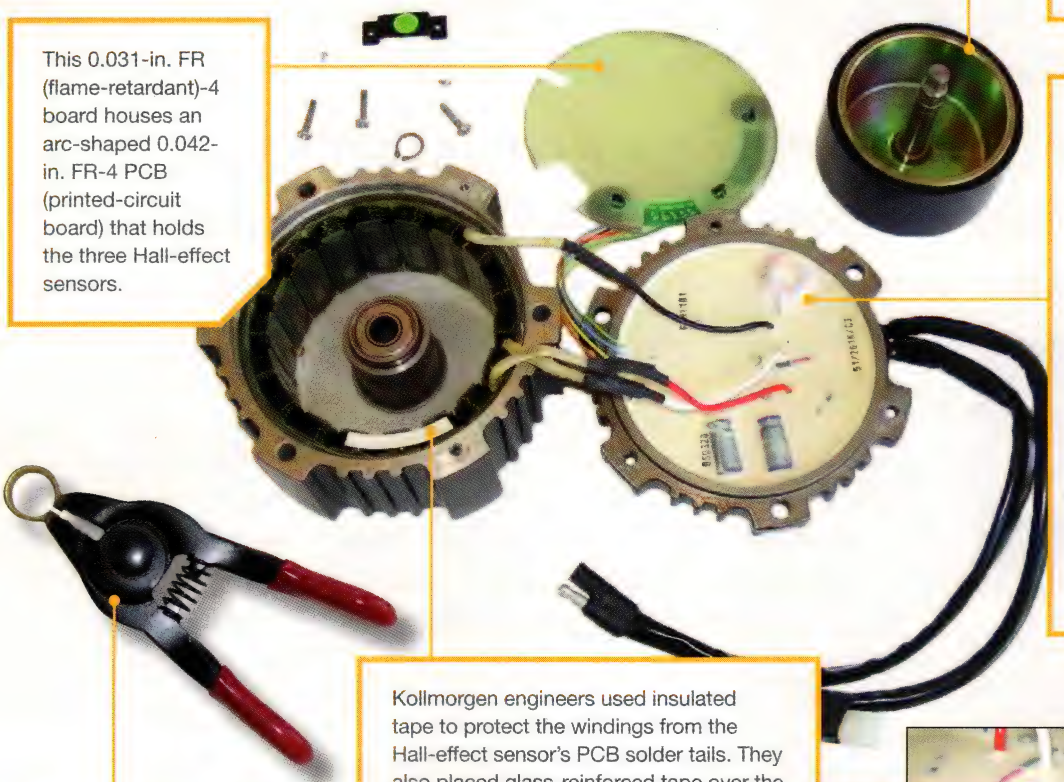
4 Technical Reference, Omega, http://bit.ly/qs9DYS.

5 Texas Instruments, www.ti.com/sensors-ca.

PRY FURTHER AT EDN.COM
Go to www.edn.com/pryingeyes for more Prying Eyes write-ups.

The 24V, 300W, BLDC Kollmorgen motor with integrated controller

Kollmorgen, a subsidiary of Danaher Corp, manufactures the 24V, 300W BLDC (brushless-dc) motor in India. A true BLDC motor, it has Hall-effect sensors that feed back the rotor position to the integrated controller. This motor, whose part number begins with CTI, is not a stepper motor, such as the CTM and CTP lines that Kollmorgen also sells; it has significant performance advantages over stepper motors. For example, its rotor incorporates closed-loop feedback and permanent magnets. Two pigtail leads come off the motor, and you feed 24V power to the thicker wires. The motor's thin harness allows you to connect a potentiometer for speed control and a switch to disable the motor. Kollmorgen most likely intended the motor for use in electric scooters and wheelchairs. Although the integrated controller eases installation, the heat it produces affects the electrolytic capacitors, reducing reliability.



The rotor is a steel shell with an outer black ring made of permanent-magnet material.

This 0.031-in. FR (flame-retardant)-4 board houses an arc-shaped 0.042-in. FR-4 PCB (printed-circuit board) that holds the three Hall-effect sensors.

The rear bell of the motor holds the BLDC controller. The two large electrolytic capacitors provide a low-impedance dc bus, preventing large switching spikes due to wiring inductance. The toroidal inductor might reduce heat-producing harmonics to the windings. A potting compound helps the motor to resist vibration and conducts heat from the components.

Kollmorgen engineers used insulated tape to protect the windings from the Hall-effect sensor's PCB solder tails. They also placed glass-reinforced tape over the switching inductor in the controller.

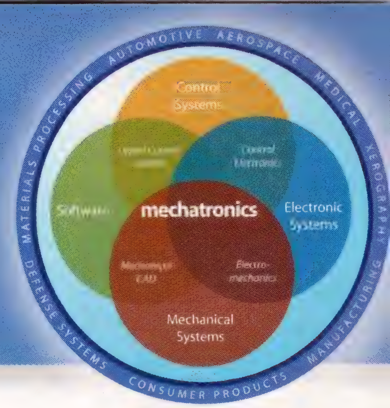
One of the pliers in the $6 Harbor Freight 96512 snap-ring pliers set eases disassembly.

An O ring seals the motor's end bell. The fit of the parts exhibits tightly held machining tolerances, even though the end bell does not hold a rotor bearing.

UBM Electronics
design news EDN Test & Measurement World

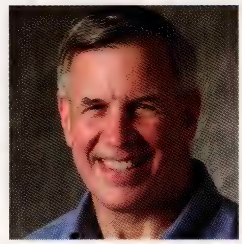
MECHATRONICS IN DESIGN

FRESH IDEAS ON INTEGRATING MECHANICAL SYSTEMS, ELECTRONICS, CONTROL SYSTEMS, AND SOFTWARE IN DESIGN



Mechatronics and building-automation systems

A mechatronic approach enhances system integration and control.



Kevin C Craig, PhD, is the Robert C Greenheck chairman in engineering design and a professor of mechanical engineering, College of Engineering, Marquette University. For more mechatronic news, visit mechatronicszone.com.

Buildings—with a carbon footprint greater than that of the transportation sector—account for more than one-third of the total energy consumption in the United States. The application of control and automation to buildings can result in significant energy savings, protect the environment, improve the health and safety of the occupants, and enhance quality of life. The most prevalent use of automation in buildings is in HVAC (heating/ventilation/air-conditioning) systems, which consume 20% of the energy in the United States.

A survey of the literature pertaining to controls for HVAC and building systems shows a lack of a systematic dynamic analysis and control design approach. The algorithms in this sector usually employ ad hoc, table-based rules, which engineers modify and improve using field experience rather than rigorous modeling and dynamic analysis. A need exists for hybrid-building systems that integrate emerging component- and control-system technologies into the broader HVAC-building system and that increase building-system energy efficiency.

An air-conditioning system must provide the cooling capacity of the system and must be as efficient as possible. The increase of enthalpy—a measure of the total energy of a thermodynamic system—across the evaporator, or the amount of heat an air-conditioning system removes from the environment, is a measure of evaporator capacity. The system coefficient of performance, a measure of system efficiency, is the ratio between the changes in enthalpy. Maximizing this value is a key system-level priority because it minimizes energy usage for a given amount of cooling. In addition, to prevent the possibility that liquid will enter the compressor inlet, it is important to maintain a prescribed level of superheated vapor at the evaporator's exit. The control of superheat and capacity are regulation problems, whereas the energy use is a minimization problem.

Because of the time scales involved, engineers use algebraic formulas to describe the mass-flow devices—that is, the compressor and the valve—and dynamics of varying degrees of complexity to describe the energy-flow devices—that is, the evaporator and the condenser heat exchanges—depending on the approach you take.

Figure 1 shows that a hierarchy of models is possible for any physical system. It is critical to strike a delicate balance between dynamic complexity and accuracy in the model. For the heat exchanger, the moving-boundary model allows the position of the phase change to vary as a function of time and lumps together the parameters in each fluid-phase region, resulting in a model of fairly low dynamic order that can accurately predict the behavior of important system outputs—for example, the superheat and the heat-exchanger pressure—that you must control to obtain efficient system operation.

As you can see, a mechatronic modeling and control design approach can have a tremendous impact on almost every modern engineering system. EDN

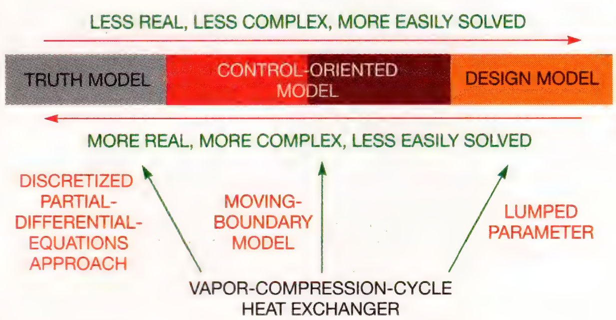
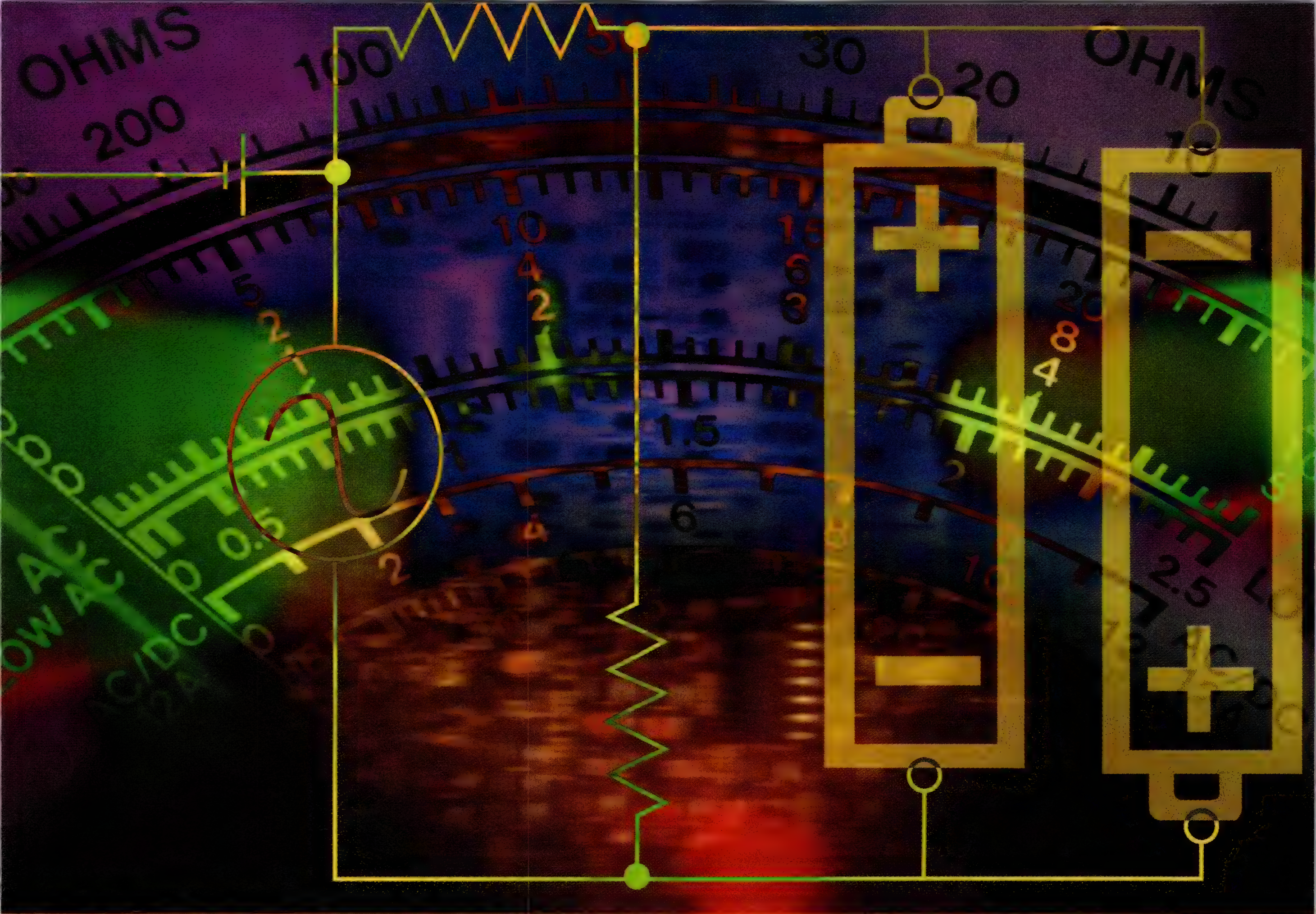


Figure 1 A hierarchy of models is possible for any physical system—from the more real, more complex, less easily solved to the less real, less complex, more easily solved. The model that is most beneficial for control design is the least complex model that still retains sufficient accuracy to capture the gross dynamic behavior of the system.



DESIGN A 100A ACTIVE LOAD TO TEST POWER SUPPLIES

BY JIM WILLIAMS • CONSULTING EDITOR

WIDEBAND RESPONSE LETS YOU TEST FOR THE TRANSIENT BEHAVIOR OF YOUR SUPPLY.

You use an active-load test circuit to ensure that a power supply for a microprocessor or for other digital loads supplies 100A transient currents. This active load can provide a dc load for a power supply, and it can rapidly switch between dc levels. These transient loads simulate the fast logic switching in the microprocessor.

Ideally, your regulator output is invariant during a load transient. In practice, however, you will encounter some variations, which become problematic if allowable operating-voltage tolerances are exceeded. You can base your active-load circuit on previous designs of wideband loads that operate at lower currents (**Reference 1**). This approach allows you to design a closed-loop, 500-kHz-bandwidth, 100A active load having linear response.

IMAGE: THINKSTOCK

Conventional active-load circuits have shortcomings (**Figure 1**). The regulator under test drives dc and switched resistive loads. Monitor the switched current and the output voltage so that you can compare the stable output voltage versus the load current under both static and dynamic conditions. The switched current is either on or off. You cannot control it in the linear region as it changes.

You can further develop the concept by including an electronic-load switch control (**Figure 2**). The input pulse switches the FET through a drive stage, generating a transient load current from the regulator and its output capacitors. The size, composition, and location of these capacitors have a profound effect on transient response. Although the electronic control facilitates high-speed switching, the architecture cannot emulate loads that are between the minimum and the maximum currents. Additionally, you are not controlling the FET's switching speed because doing so introduces wideband harmonics into the measurement that may corrupt the oscilloscope display.

AT A GLANCE

- Use active loads to test your power supplies.
- Using wide-bandwidth circuitry allows fast transient response.
- Trim the circuit to obtain the cleanest load-step signals.
- Minimize the inductance in the high-current path.
- Verify the measurements in a separate test setup.

TRANSIENT GENERATOR

Placing Q_1 within a feedback loop allows true, linear control of the load tester (**Figure 3**). You can now linearly control Q_1's gate voltage, allowing you to set an instantaneous transient current at any point and to simulate nearly any load profile. Feedback from Q_1's source to control amplifier A_1 closes a control loop around Q_1, stabilizing its operating point. The instantaneous input-control voltage and the value of the current-sense resistor set Q_1's current over a wide bandwidth. You use the dc-load-set potentiometer to bias A_1 to the conduction threshold of Q_1. Small variations in A_1's output result in large current changes in Q_1, meaning that A_1 need not supply large output excursions. The fundamental speed limitation is the small-signal bandwidth of the amplifier. As long as the input signal stays within this bandwidth, Q_1's current waveform is identical in shape to A_1's input control voltage, allowing linear control of the load current. This versatile capability permits you to simulate a wide variety of loads.

You can improve this circuit by adding some components (**Figure 4**). A gate-drive stage isolates the control amplifier from Q_1's gate capacitance

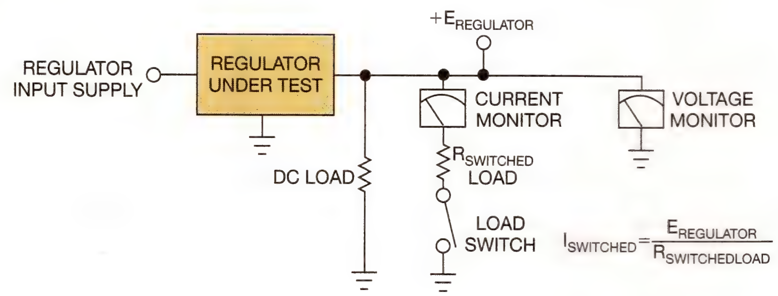


Figure 1 This conceptual regulator-load tester includes switched and dc loads and monitors voltage and current. The resistor values set dc and switched-load currents.

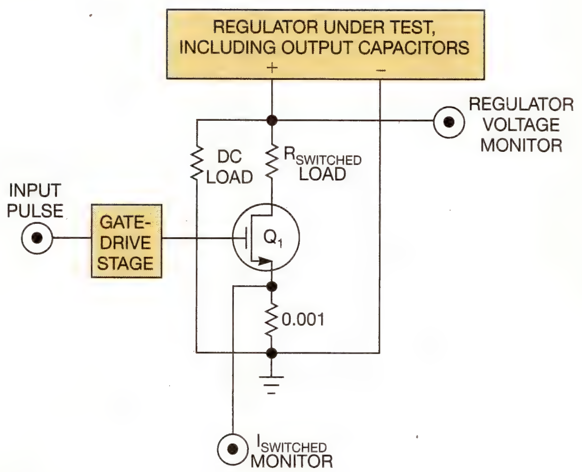


Figure 2 A conceptual FET-based load tester permits step loading. Switched current is either on or off; there is no controllable linear region.

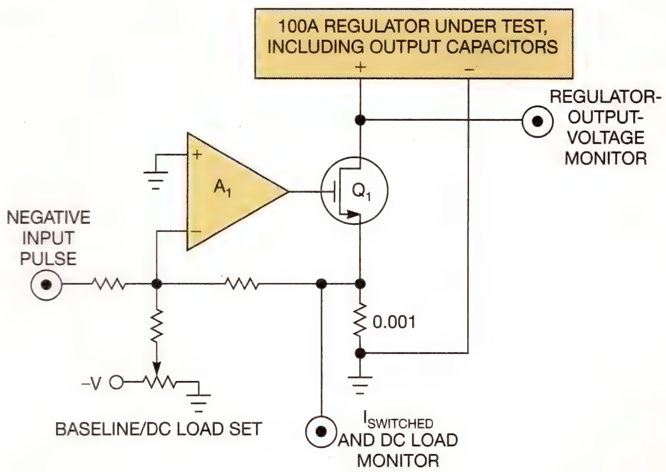


Figure 3 A feedback-controlled load-step tester allows continuous FET-conductivity control.

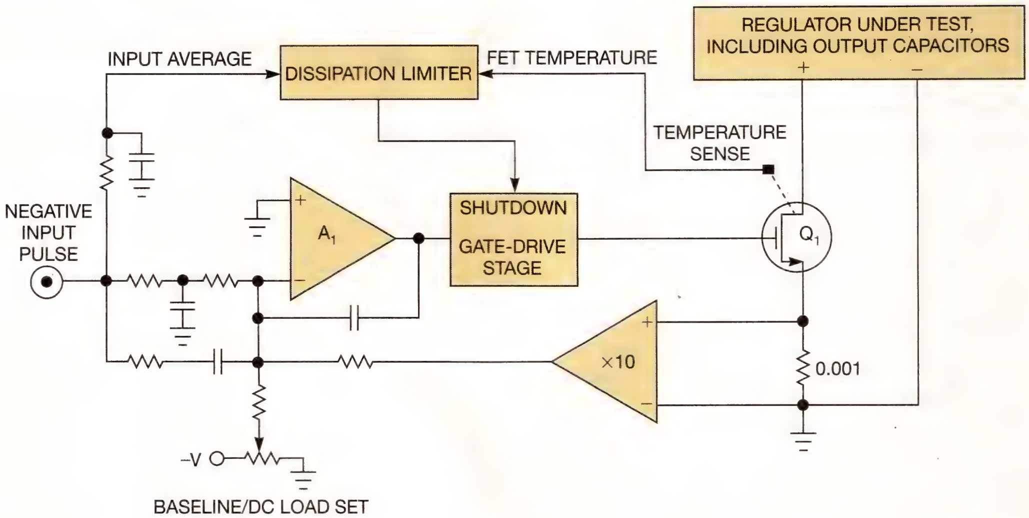


Figure 4 Adding a differential amplifier provides high-resolution sensing across a 1-mΩ shunt resistor. A dissipation limiter shuts down the gate drive. Added capacitors tailor the bandwidth and optimize the loop response.

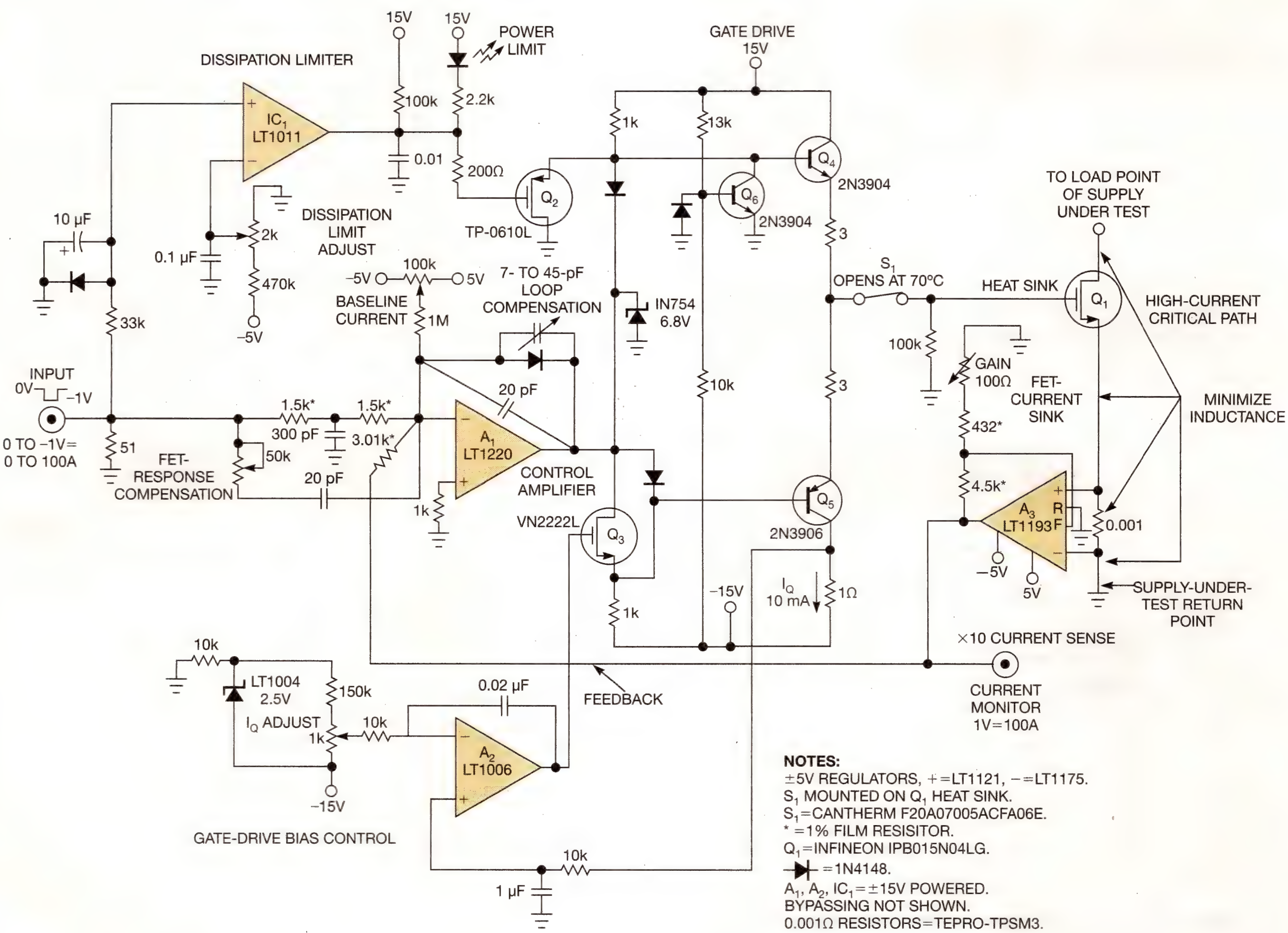
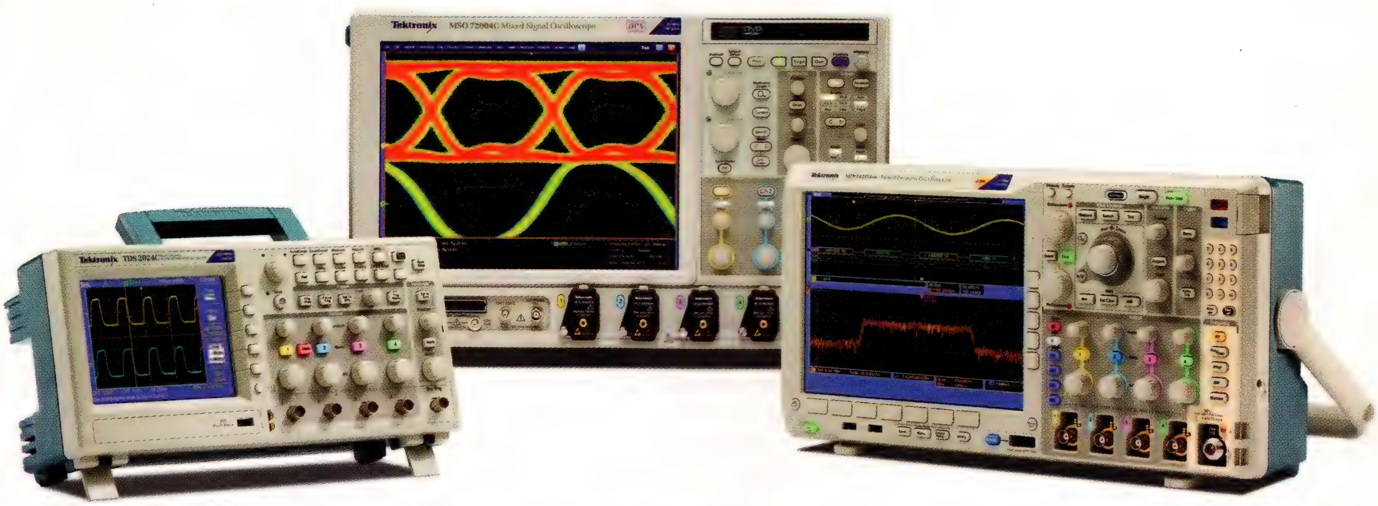


Figure 5 You can derive a detailed active-load schematic from the conceptual design.

Oscilloscopes Don't Change the World. Engineers Do.



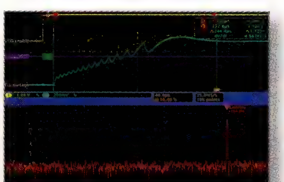
Basic Visualization – 40 to 500 MHz

Performance Analysis – DC to 80 GHz

Bench Debug – 100 MHz to 1 GHz

No wonder so many trust Tektronix oscilloscopes, the world's standard for innovation.

Tektronix offers the broadest portfolio of oscilloscopes to debug and test tomorrow's designs, today. Start with Tektronix Basic oscilloscopes. Fast, familiar and affordable, they're what you know and trust. Our Bench oscilloscopes—including the world's first Mixed Domain Oscilloscope—provide next-level productivity, with the feature-rich tools you need to debug today's complex mixed signal designs. And for those who demand the industry's best signal fidelity, verification and characterization capabilities, our Performance oscilloscopes help you shorten your design cycles.



See why so many engineers worldwide rely on Tektronix oscilloscopes.

www.tektronix.com/worldstandard

Tektronix®

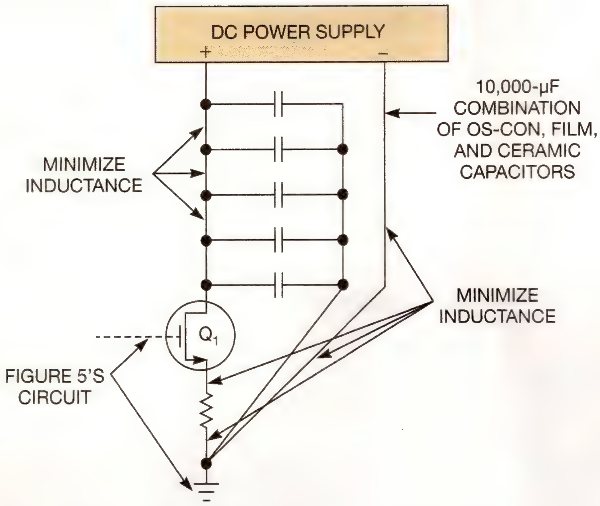


Figure 6 The test fixture for dynamic response has massive, broadband bypassing and a low-inductance layout. This setup provides low-loss, high-current power to Q_1.

CAPACITORS CAN BE ADDED TO THE MAIN AMPLIFIER TO TAILOR THE BANDWIDTH AND OPTIMIZE THE LOOP RESPONSE.

to maintain the amplifier's phase margin and provide low delay and linear current gain. A gain-of-10 differential amplifier provides high-resolution sensing across the 1-mΩ current-shunt resistor. You can design a power-dissipation limiter that acts on the averaged input value and Q_1's temperature. It shuts down the FET's gate drive to preclude excessive heating and subsequent destruction. Capacitors can be added to the main amplifier to tailor the bandwidth and optimize the loop response.

You can develop a detailed schematic based on these concepts (**Figure 5**). The main amplifier, A_1, responds to dc and pulse inputs. You also send it a feedback signal from A_3 that represents load current. A_1 sets Q_1's conductivity through the Q_4/Q_5 gate-drive stage, which is actively biased using A_2. The voltage drop across the gate drive's input diodes would be high enough to fully turn on Q_4 and Q_5. To prevent this overdrive, reduce the voltage across the lower diode with Q_3. Amplifier A_2 determines the gate-drive-stage bias by comparing Q_5's averaged collector current with a reference and controlling Q_3's conduction, thus closing a loop. That loop keeps the voltage drop

VERIFYING CURRENT MEASUREMENT

Theoretically, Q_1's source and drain current are equal. Realistically, they can differ due to the effects of residual inductances and the 28,000-pF gate capacitance. A_3's indicated instantaneous current could be erroneous if these or other terms come into play. You can verify that the source and the drain currents are equivalent (Figure A). Add a top-side, 1-mΩ shunt and a gain-of-10 differential amplifier to duplicate the circuit's bottom-side current-sensing section. The results should eliminate concern over Q_1's dynamic-current differences (Figure B). The two 100A pulse outputs are identical in amplitude and shape, promoting confidence in the circuit's operation.

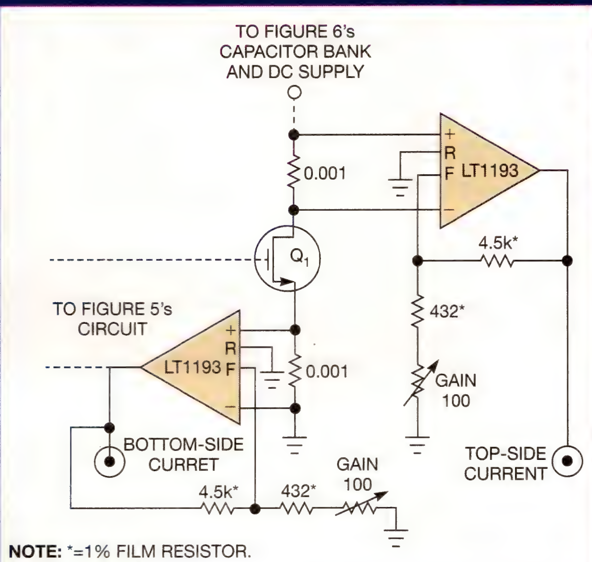


Figure A Use this arrangement for observing Q_1's top and bottom dynamic currents.

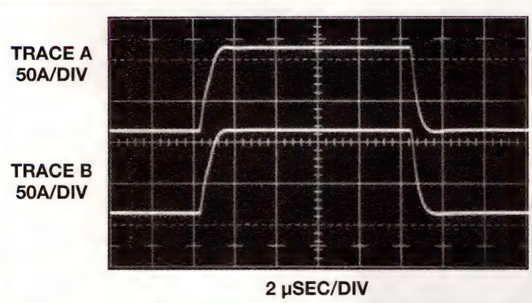


Figure B Q_1's top (Trace A) and bottom (Trace B) currents show identical characteristics despite high-speed operation.

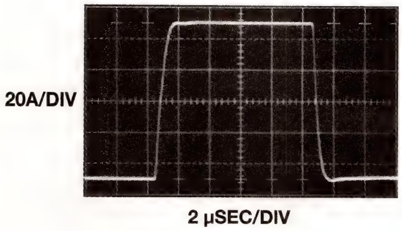


Figure 7 When you optimize the dynamic response, you get an exceptionally pure 100A current pulse.

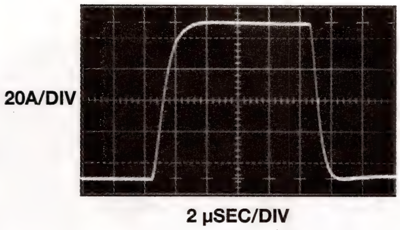


Figure 8 The response becomes overdamped if you set an excessive feedback-capacitor value for A_1.

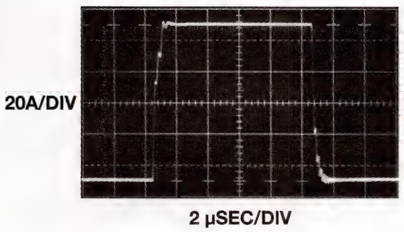


Figure 9 An inadequate feedback-capacitor value for A_1 decreases the transition time but promotes instability. Further capacitor reduction causes oscillation.

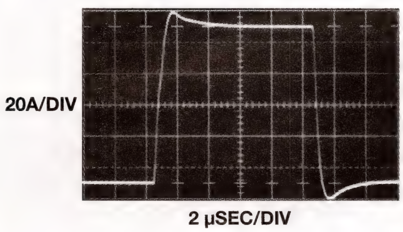


Figure 10 Overdoing the FET's response compensation results in corner peaking.

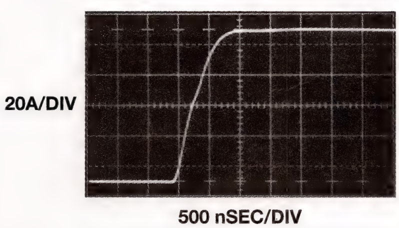


Figure 11 By optimizing the dynamic trims, the circuit gets a 650-nsec rise time, corresponding to a 540-kHz bandwidth.

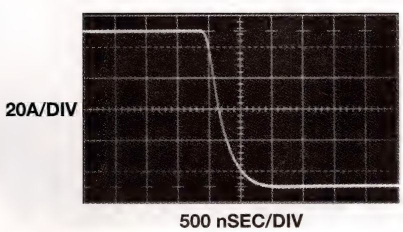


Figure 12 The optimized trims yield a 500-nsec fall time.

across the bases of Q_4 and Q_5 to a value well under 1.2V, and servos that value until Q_4 and Q_5 have a 10-mA average collector-bias current.

The duty cycle of the load overheats if it is on for too long. You can fashion a protection circuit with techniques that high-power-pulse-generator designers use (**references 2, 3, and 4**). Feed comparator IC_1 the average input-voltage value. It compares that voltage to a reference voltage set with the dissipation-limit-adjust potentiometer. If the input duty cycle exceeds this limit, comparator IC_1 turns off the FET gate drive through Q_2. Thermal switch S_1 provides further protection. If Q_1's heat sink gets too hot, S_1 opens and disconnects the gate-drive signal. By diverting Q_4's bias voltage, transistor Q_6 and the zener diode prevent Q_1 from turning on if the −15V supply is not present. A 1-kΩ resistor on A_1's positive input prevents amplifier damage should you lose the 15V power supply.

Trimming optimizes the dynamic response, determines the loop's dc baseline idle current, sets the dissipation limit, and controls the gate drive's stage bias. The dc trims are self-explanatory. The loop-compensation and FET-response ac trims at A_1 are subtler. Adjust them for the best compromise

INSTRUMENTATION CONSIDERATIONS

The pulse-edge rates in the main article are not particularly fast, but high-fidelity response requires some diligence. In particular, the input pulse must be cleanly defined and devoid of parasitics, which would distort the circuit's output-pulse shape. A_1's 2.1-MHz input RC (resistance/capacitance) network filters the pulse generator's preshoot, rise-time, and pulse-transition aberrations, which are well out of band. These terms are not of concern. Almost all general-purpose pulse generators should perform well.

A potential offender is excessive tailing after transitions. Meaningful dynamic testing requires a rectangular pulse shape, flat on the top and the bottom within 1 to 2%. The circuit's input band-shaping filter removes the aforementioned high-speed-transition-related errors but does not eliminate lengthy tailing in the pulse flats. You should check the pulse generator for this issue with a well-compensated probe at the circuit input. The oscilloscope should register the desired flat-top- and flat-bottom-waveform characteristics. In making this measurement, if high-speed-transition-related events are bothersome, you can move the probe to the bandlimiting 300-pF capacitor. This practice is defensible because the waveform at this point determines A_1's input-signal bandwidth.

Some pulse-generator output stages produce a low-level dc offset when their output is nominally at its 0V state. The active-load circuit processes such dc potentials as legitimate signals, resulting in a dc-load baseline-current shift. The active load's input scale factor of 1V=100A means that a 10-mV zero-state error produces 1A of dc baseline-current shift. A simple way to check a pulse generator for this error is to place it in external-trigger mode and read its output with a DVM (digital voltmeter). If offset is present, you can account for it by nullifying it with the circuit's baseline-current trim. You could also use a different pulse generator.

Keep in mind parasitic effects due to probe grounding and instrument interconnection. At pulsed 100A levels, you can easily induce parasitic current into "grounds" and interconnections, distorting displayed waveforms. Use coaxially grounded probes, particularly at A_3's output-current monitor and preferably anywhere else.

It is also convenient and common practice to externally trigger the oscilloscope from the pulse generator's trigger output. There is nothing wrong with this practice; in fact, it is a recommended approach for ensuring a stable trigger as you move probes between points. This practice does, however, potentially introduce ground loops due to multiple paths between the pulse generator, the circuit, and the oscilloscope. This condition can falsely cause apparent distortion in displayed waveforms. You can avoid this effect by using a trigger isolator at the oscilloscope's external-trigger input. This simple coaxial component typically comprises isolated ground and signal paths, which often couple to a pulse transformer to provide a galvanically isolated trigger event. Commercial examples include the Deerfield Laboratory (www.deerfieldlab.com) 185 and the Hewlett-Packard (www.hp.com) 11356A. Alternatively, you can construct a trigger isolator in a small BNC-equipped enclosure (Figure A).

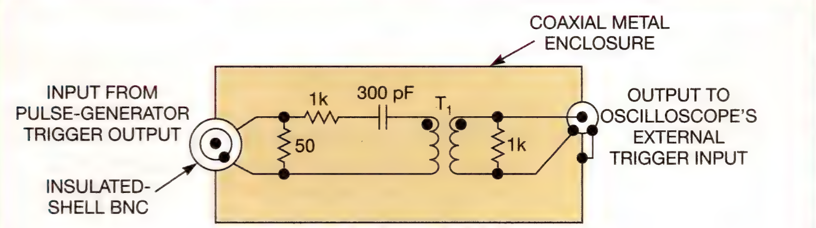


Figure A You can make a trigger isolator that floats input BNC's ground using an insulated-shell BNC connector. A capacitively coupled pulse transformer avoids loading input, maintains isolation, and delivers the trigger to the output. A secondary resistor on T_1 terminates ringing.

between loop stability, edge rate, and pulse purity. You can use A_1's loop-compensation trimming capacitor to set the roll-off for maximum bandwidth and accommodate the phase shift that Q_1's gate capacitance and A_3 introduce. The FET-response adjustment partially compensates Q_1's inherent nonlinear-gain characteristic, improving the front and rear pulses' corner fidelity (see **sidebar** "Trimming procedure," with the online version of this article at www.edn.com/110922df).

CIRCUIT TESTING

You initially test the circuit using a fixture equipped with massive, low-loss, wideband bypassing (**Figure 6**). It is important to do an exceptionally low-inductance layout in the high-current path. Every attempt must be made

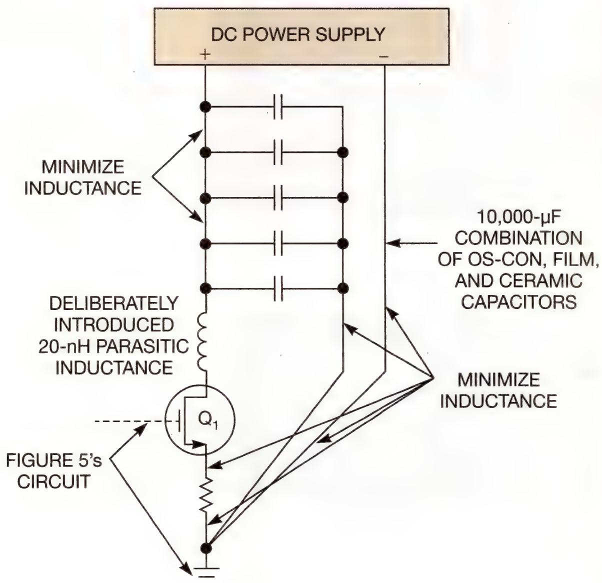


Figure 13 You can deliberately introduce a parasitic, 20-nH inductance to test layout sensitivity.

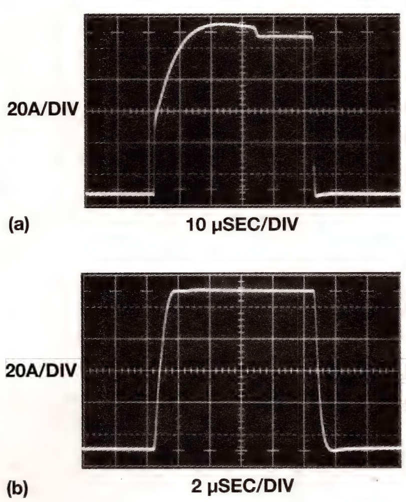


Figure 14 A 20-nH-inductance, 1.5× 0.075-in., flat-copper, braided wire completely distorts (a) the optimized response (b). Note the five-times-horizontal-scale change between a and b.

to minimize inductance in the 100A path. You should get good results after you properly trim the circuit if you minimize inductance in the high current path (**Figure 7**). The 100A-amplitude, high-speed waveform is pure, with barely discernible top-front and bottom-rear corner infidelities (see **sidebars** "Verifying current measurement" and "Instrumentation considerations").

To study the effects of ac trim on the waveform, you must perform deliberate misadjustments. An overdamped response is typical of excess A_1 feedback capacitance (**Figure 8**). The current pulse is well-controlled, but the edge rate is slow. Inadequate feedback capacitance from A_1 decreases the transition time but promotes instability (**Figure 9**). Further reducing the trim capacitance causes loop oscillation because the loop's phase shift causes a significant phase lag in the feedback. Scope photos of uncontrolled 100A loop oscilla-

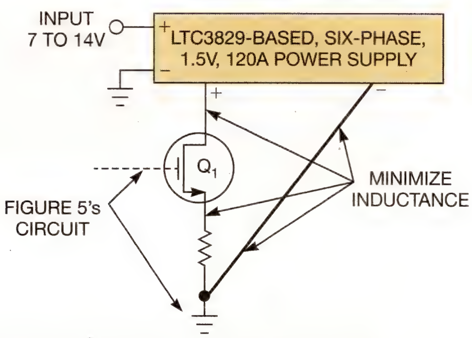


Figure 15 Use low-impedance connections to test a six-phase, 120A buck regulator.

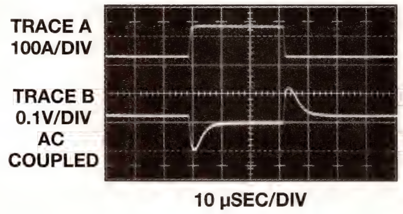


Figure 16 The regulator's response to a 100A pulsed load (Trace A) is well-controlled on both edges (Trace B).

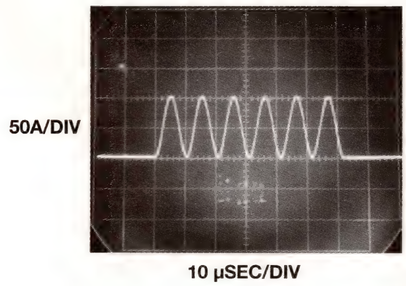


Figure 17 You can use the circuit to create a 100-kHz, 100A-sine-wave load.

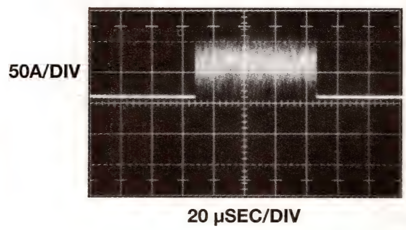


Figure 18 The active-load circuit sinks 100A p-p in response to a gated random-noise input.

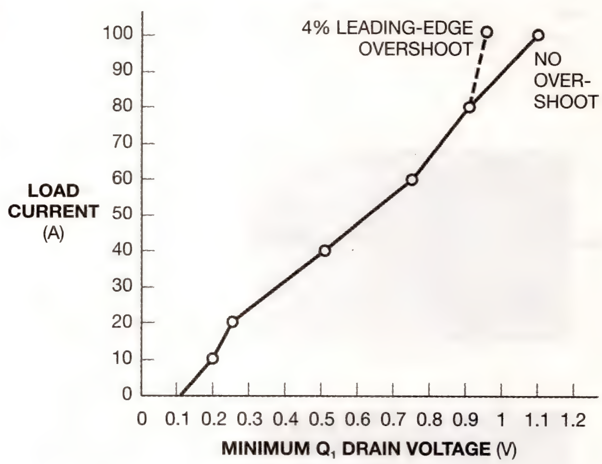


Figure 19 Active-load characteristics feature small current-accuracy and regulation errors. The bandwidth mildly retards at low currents. The compliance voltage is less than 1V at 100A with 4% leading-edge overshoot and 1.1V with no overshoot.

TABLE 1 ACTIVE-LOAD CHARACTERISTICS

Current accuracy (referred to input)	1% full-scale
Temperature drift	100 ppm/°C of reading +20 mA/°C
Current regulation versus supply	Greater-than-60-dB power-supply-rejection ratio
Bandwidth	540 kHz at 100A with a rise time of 650 nsec, 435 kHz at 10A with a rise time of 800 nsec
Compliance voltages for full output current	0.95V minimum (see Figure 19); 70°C Q_1 thermal-dissipation limiter sets maximum

tion are unavailable. The event is too thrilling to document. Overdoing the FET's response compensation causes peaking in the corners of the waveform (**Figure 10**). Restoring the ac trims to nominal values causes a 650-nsec rise time, equivalent to a 540-kHz bandwidth, on the leading edge (**Figure 11**). Examining the trailing edge under the same conditions reveals a somewhat-faster 500-nsec fall time (**Figure 12**).

LAYOUT EFFECTS

If parasitic inductance is present in the high-current path, your design cannot remotely approach the previous responses. You can deliberately place a tiny, 20-nH parasitic inductance in Q_1's drain path (**Figure 13**), which will cause an enormous waveshape degradation deriving from the inductance and the loop's subsequent response (**Figure 14a**). A monstrous error dominates the leading edge before recovery occurs at the middle of the pulse's top. Additional aberration is evident in the falling edge's turn-off. The **figure**'s horizontal scale is five times slower than the optimized response (**Figure 14b**). The lesson is clear: High-speed 100A excursions do not tolerate inductance.

REGULATOR TESTING

After you address the compensation and layout issues, you can test your power-supply regulator (**Figure 15**). The six-phase, 120A Linear Technology Corp (www.linear.com) LTC1675A buck regulator acts as a demonstration board. The test circuit generates the 100A load pulse (Trace A of **Figure 16**). The regulator maintains a well-controlled response on both edges (Trace B of **Figure 16**). The active load's true linear response and high bandwidth permit wide-ranging load-waveform characteristics. Although the step-load pulse in **Figure 16** is the commonly desired test, you can generate any load profile. A burst of 100A, 100-kHz sine waves is an example (**Figure 17**). The response is crisp, with no untoward dynamics despite the high speed and current. You could form a load even from an 80-µsec burst of 100A p-p noise (**Figure 18**). The load circuit has high accuracy, compliance, and regulation specifications (**Figure 19** and **Table 1**). EDN

REFERENCES

1 Williams, Jim, "Load Transient Response Testing for Voltage Regulators," Application Note 104, Linear Technology Corp, October 2006, http://bit.ly/p5q2AD.

2 "Overload Adjust," *HP-214A Pulse Generator Operating and Service Manual*, Hewlett-Packard, figures 5 through 13.

3 "Overload Relay Adjust," *HP-214A Pulse Generator Operating and Service Manual*, Hewlett-Packard, 1964, pg 5.

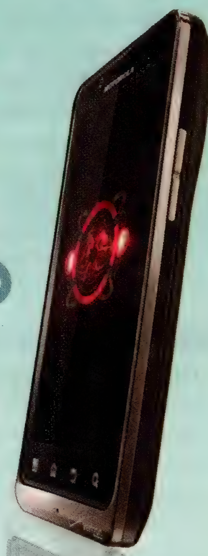
4 "Overload Detection/Overload Switch," *HP-214B Pulse Generator Operating and Service Manual*, Hewlett-Packard, March 1980, pg 8.

AUTHOR'S BIOGRAPHY

Jim Williams was a staff scientist at Linear Technology Corp, where he specialized in analog-circuit and instrumentation design. He served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology (Cambridge, MA). He enjoyed sports cars, art, collecting antique scientific instruments, sculpture, and restoring old Tektronix oscilloscopes. A long-time EDN *contributor, Williams died in June 2011 after a stroke.*

MODERN SENSORS GREATLY ENHANCE CONSUMER-ELECTRONIC-SYSTEM PERFORMANCE

BY STEVE TARANOVICH • CONTRIBUTING TECHNICAL EDITOR



You can expect a large evolutionary trend in sensors over the next few years. Demand is strong for more precise navigation technology, especially for indoor asset and global tracking. This technology will significantly affect the inertial- and motion-sensor consumer markets, which include accelerometers, gyroscopes, and magnetometers in mobile phones, tablets, game stations, laptops, and other devices. Addressing this trend, this article is the first of a two-part series on sensors in consumer systems (see **sidebar** "Perspectives on modern sensors"). It explores the various sensor options and how to properly link the analog world of sensors and their conditioning circuits to the digital world of processing data and adding intelligence. It also examines the inherent trade-offs for some popular options and discusses discrete approaches versus highly integrated approaches. A one-size-fits-all approach may sometimes fail to attain the performance parameters that some systems need. Although designers may in many cases gravitate to more highly integrated approaches due to time-to-market constraints, these approaches may not lead to a design that consumers will flock to the stores to purchase. Designers should balance performance and features with size and cost to make a successful product for the consumer market.

IMAGES: ISTOCKPHOTO

WITH THE ADOPTION OF SENSORS AND CONNECTIVITY, CONSUMER DEVICES HAVE UNDERGONE A REVOLUTION: THEY ARE NO LONGER ONE-WAY, ISOLATED ISLANDS. THEY NOW INCLUDE USER AND ENVIRONMENTAL AWARENESS AND INTERACTIVITY, AS WELL AS CONNECTIVITY WITH SURROUNDING SYSTEMS AND THE INTERNET.

Sensors live in the analog world of touch, temperature, image, light, position, motion, and pressure, in which mobile phones, smartphones, notebooks, MP3 players, and game consoles are ubiquitous. The most popular types of sensors help to enliven your world of entertainment, information technology, communication, home appliances, and other product markets. Most touch sensor technologies in today's designs are either capacitive or resistive. Capacitive sensors are suitable for a range of sensing applications, such as keypads, rotators, or buttons, whereas resistive-touchscreen sensors use a four-wire resistive technology, usually with built-in ADCs, to offer both ease of design and greater flexibility to touchscreen applications.

AT A GLANCE

- A one-size-fits-all approach may sometimes fail to attain the performance parameters that some systems need.
- The most popular types of sensors help to enliven your world of entertainment, information technology, communication, home appliances, and other product markets.
- Capacitive sensors are suitable for a range of sensing applications, such as keypads, rotators, or buttons.
- Resistive-touchscreen sensors use a four-wire resistive technology, usually with built-in ADCs, to offer both ease of design and greater flexibility to touchscreen applications.

CAPACITIVE TOUCHSCREENS

A capacitive-touchscreen panel comprises an insulator, such as glass, coated with a transparent conductor, such as ITO (indium tin oxide). Because the human body is also an electrical conductor, touching the surface of the screen results in a distortion of the screen's electrostatic field, which is measurable as a change in capacitance.

When choosing a touchscreen controller, you should consider several aspects, including the accuracy of the CDC (capacitance-to-digital converter); the unit's noise-handling ability, which the digital filter of the ADC usually handles; its environmental compensation; and the advanced algorithms in its host processor or CDC chip, which provide WinCE (Windows Compact Edition) or Linux driver and software capabilities. These features allow you to develop a system that accurately detects finger presence, motion, and intended activity on the touchscreen.

STMicroelectronics offers highly integrated capacitive and resistive, multiple-channel touchscreen solutions with controllers that interface seamlessly to a host processor using the S-Touch series of controllers for touch-key and touchscreen applications. The company's portfolio of sensors also includes MEMS (microelectromechanical-system) motion sensors for measuring motion, acceleration, inclination, and vibration; proximity detectors for metal-body-proximity sensing; and analog and digital temperature sensors.

Touchscreen controllers typically use a 24-bit converter because they need to digitize only small levels of capacitance. One such converter is Analog Devices' 24-bit, two-channel AD7746 CDC. The device measures capacitance that connects between the on-chip excitation source and the on-chip sigma-delta modulator's input. An on-chip square-wave excitation signal is applied on the capacitance of the touchscreen during the conversion, and the modulator continuously samples the charge through the capacitor. The digital filter processes the modulator's output, which is a stream of zeros and ones containing the information in zero and one density. The CDC then scales the data from the digital filter, applying the calibration coefficients. You can read the final result through the serial interface, which sends it to an external host processor through a serial bus (**Figure 1**).

When considering a device's environmental compensation, keep in mind that ambient-temperature changes can cause fluctuations in stray capacitance. You can use an external temperature sensor for compensation, such as the

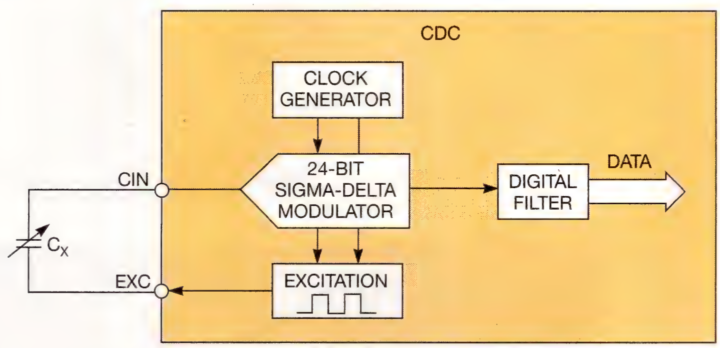


Figure 1 Analog Devices' 24-bit, two-channel AD7746 CDC measures touchscreen capacitance that connects between the on-chip excitation source and the on-chip sigma-delta modulator's input. An on-chip square-wave excitation signal is applied on the capacitance of the touchscreen during the conversion, and the modulator continuously samples the charge through the capacitor.

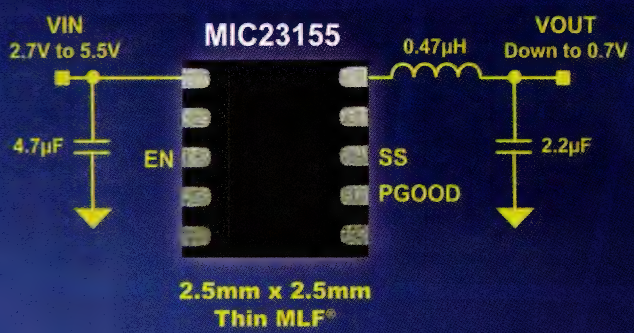
TABLE 1 PASSIVE AND ACTIVE TEMPERATURE SENSORS

	Thermocouple	RTD	Thermistor	Semiconductor
Temperature range (°C)	–184 to +2300	–200 to +850	0 to 100	–55 to +150
Accuracy/ linearity	High accuracy and repeatability	Fair linearity	Poor linearity	1°C linearity, 1°C accuracy
Comments	Needs cold-junction compensation; has low-voltage output	Requires excitation; is low cost	Requires excitation; has high sensitivity	Requires excitation; 10-mV/K, 20-mV/K, or 1-μA/K typical output

Extend Your Battery Life with Micrel "Green Power" Regulators

HyperLight Load® Synchronous Buck

- ▶ Ultra High Efficiency — > 93%
- ▶ Ultra Small Size — 2.5 x 2.5mm
- ▶ Ultra Powerful — 2A
- ▶ Ultra Fast — 4MHz



MIC23155 delivers extremely high efficiency for portable products and green home/office appliances. Micrel's HyperLight Load® Regulators save precious power over the entire load range for 'green' devices.

The MIC23155 features internal MOSFETs able to deliver up to 2A output current while consuming just 23µA of quiescent current inside an ultra-small 2.5mm x 2.5mm Thin MLF® package.

For more information, contact your local Micrel sales representative or visit Micrel at: www.micrel.com/ad/mic23155.

Ideal for use in:

- Mobile handsets
- Portable media/MP3 players
- Portable navigation devices (GPS)
- WiFi/WiMax/WiBro modules
- Solid State Drives/Memory
- Wireless LAN cards
- Portable applications

MICREL®
Innovation Through Technology®
www.micrel.com

base-to-emitter voltage junction of a transistor; however, you must be careful to compensate for the PCB's (printed-circuit board's) resistance from the transistor to the chip input.

RESISTIVE TOUCHSCREENS

A resistive-touchscreen panel includes several layers, the most important of which are two thin, electrically conductive layers separated by a narrow gap. When an object, such as a finger, presses on a point on the panel's outer surface, the two metallic layers connect at that point. The panel then behaves as a pair of voltage dividers with connected outputs, causing a change in the electrical current, which the panel registers as a touch event and sends to the controller for processing.

When choosing a resistive-touchscreen controller, use many of the same criteria you would use in selecting the capacitive-touchscreen controller. These criteria include the accuracy of the ADC; the noise-handling ability—for which digital filtering can occur on the controller chip, the host processor, or both; environmental compensation; and the ability to use advanced algorithms, which, in resistive units' case, usually reside in the host processor and enable WinCE or Linux driver and software features. A 12-bit ADC is typically accurate enough, and some devices provide ratiometric-conversion tech-

PERSPECTIVES ON MODERN SENSORS

Sensor manufacturers are adding features to consumer devices through a combination of appropriate hardware integration, efficient foundry processes, larger wafers, and clever software innovations. These features will revolutionize the consumer-electronics industry. The perspectives of some key participants in the market follow.

JALINOUS ESFANDYARI,
PhD, *MEMS (microelectromechanical-system)-product marketing manager, STMicroelectronics*
Perspective: "Sensor-fusion solutions are the trend. Sensors now integrate at least six degrees of freedom [an accelerometer with three axes and a gyro with three axes], which makes up an IMU [inertial-measurement unit]. By adding a magnetic sensor and a compass with three axes, you can minimize drift over time and temperature. So, nine degrees of freedom in one package is achievable for location-based and dead-reckoning applications. Even though [you can also integrate] a microcontroller into the package for digital filtering to take care of drift, noise, and distortion, [you need to weigh] trade-offs looking at size versus performance. Sometimes, separating some of the integrated parts might make it easier to arrange on a PCB [printed-circuit board]—for example, keeping the magnetic sensor away from a speaker magnet or an image sensor to avoid problems."

TIM KALTHOFF,
fellow and chief technologist in the high-performance-analog division, Texas Instruments
Perspective: "In general, microminiaturization of sensors, through MEMS-technology advances, now allows designers to use sensors in applications they never would have considered in the past due to size and cost."

MICHAEL STEFFES,
application manager, Intersil
Perspective: "The online-design tools are getting better at getting you close to the end solution." National Semiconductor's Webench is a great example of such a tool (Reference A).

SAJOL GHOSHAL,
business-unit manager for advanced platform products, TAOS (Texas Advanced Optoelectronic Solutions)
Perspective: "Energy management is the key in products such as smartphones. Light sensors can turn an LED off or lower its intensity, which results in a big savings in power and, thus, longer battery life. Batteries needed recharging in two hours in the past, and now we can give users eight to nine hours. Using CMOS technology and simple algorithms achieves this goal."

KERRY GLOVER,
application manager, TAOS
Perspective: "Higher integration is coming, with LED drivers having the light sensors on the same chip. [This approach will give designers a faster time to market.]"

OLEG STECIW,
senior marketing manager for optical-sensing products, Intersil
Perspective: "We are not seeing many discrete implementations. Light sensors with integrated transimpedance amplifiers, ADCs, and series digital buses, such as I^2C [inter-integrated circuit] and SMBus [system-management bus], improve not only performance but also critical time to market. Older-generation light-sensor algorithms did not work well, and users would tend to disable the function, but software has greatly improved, and studies show 30 to 40% power savings in backlighting."

Software will affect designers' choices. They can achieve intelligence and enhanced performance in software—sometimes at the expense of hardware. Examples include filtering, comparing, timing, and virtual touchscreen switches and knobs. Designers will have tough choices to make, depending on the market they are focusing on, but these choices will be available to them as sensor trends continue to evolve over the next few years.

REFERENCE

A Rako, Paul, "Single-op-amp Sallen-Key filters, filter fanatics," *EDN*, April 20, 2011, http://bit.ly/nCEa3n.

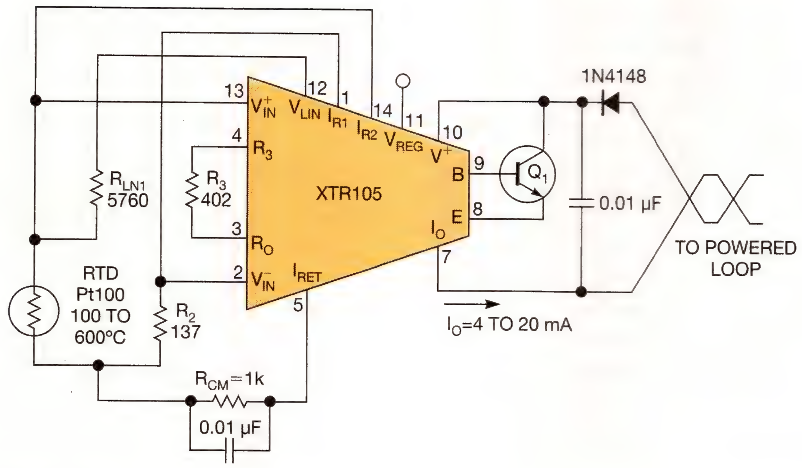


Figure 2 Texas Instruments' monolithic, 4- to 20-mA, two-wire XTR105 current transmitter has two precision current sources. Possible choices for Q_2 include 2N4922, TIP29C, and TIP31C, which come in TO-225, TO-220, and TO-220 packages, respectively.

niques, which provide noise immunity and tolerance of long leads. The binary result is free of reference drift errors because the excitation source is driven by the ADC reference. To implement environmental compensation for resistive touchscreens, you can use either on-chip measurement to sense fluctuations in temperature that can affect the data converter or off-chip temperature monitoring to compensate for resistive changes with ambient temperature.

One example of a resistive-touch-screen controller, Maxim's low-power MAX11811, works with power-sensitive, handheld systems employing advanced low-voltage processors. The device contains a 12-bit SAR (successive-approximation-register) ADC and a multiplexer to interface with a resistive-touchscreen panel. A digital serial interface provides communications. The MAX11811 includes digital preprocessing of the touchscreen's measurements, reducing bus-loading and application-processor requirements.

TEMPERATURE SENSORS

Passive temperature sensors include RTDs (resistance-temperature detectors), thermocouples, and thermistors. You can usually interface RTDs and thermistors to an amplifier circuit to provide a voltage that is proportional to temperature. **Table 1** compares passive and active temperature sensors.

RTDs are accurate and repeatable, have low drift error, and have a temperature range of −200 to +850°C. Due to nonlinearities, these sensors

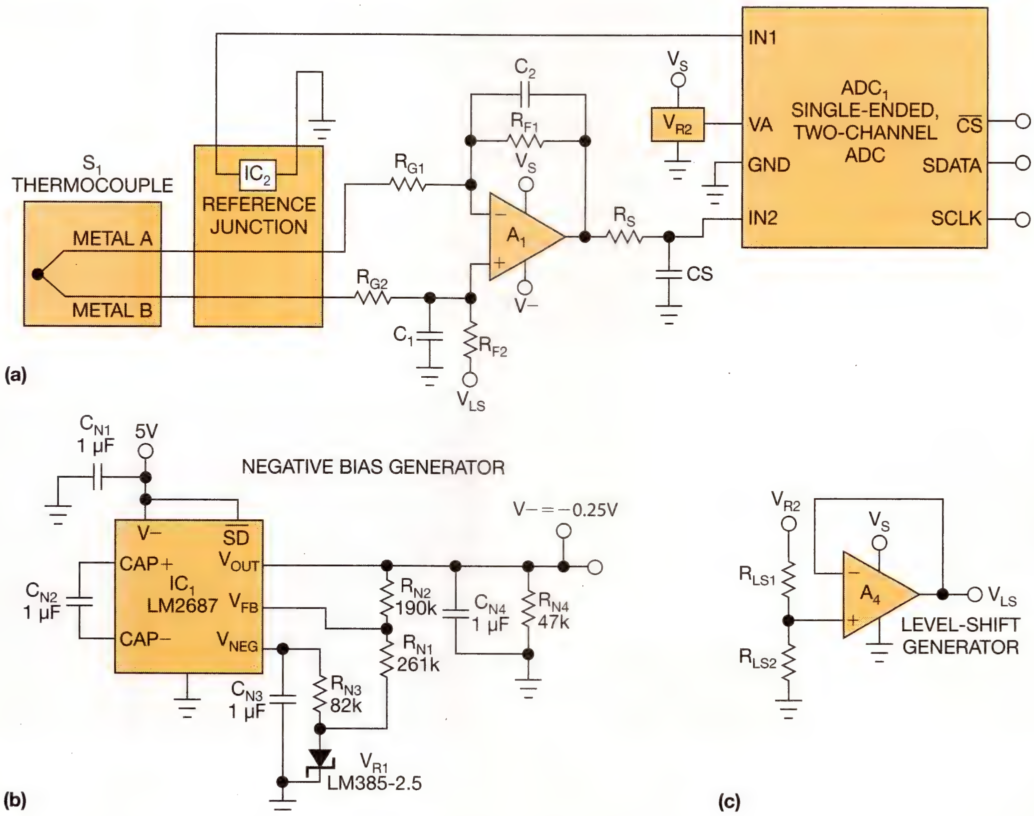


Figure 3 A differential amplifier amplifies the thermocouple voltage, driving a single-ended ADC (a). The negative bias generator (b) and level-shift generator (c) are optional (courtesy National Semiconductor).

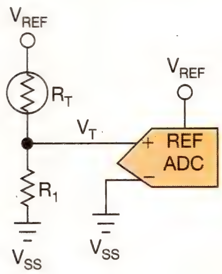


Figure 4 You can use NTC thermistors for temperature measurement as resistance thermometers, but calibration is necessary if the application operates over large changes in temperature (courtesy Maxim Integrated Products).

also need linearization, which you can implement using a look-up table in a microcontroller. These sensors are usually in a bridge configuration with differential outputs to help minimize lead-resistance errors. A difference amplifier or an instrumentation amplifier can be used to amplify and filter these sensors.

Texas Instruments, however, offers an integrated approach in its monolithic, 4- to 20-mA, two-wire XTR105 current transmitter, which has two precision current sources. It provides complete current excitation for platinum-RTD temperature sensors and bridges, instrumentation amplifiers, and current output circuitry on one IC. Engineers usually run the 4- to 20-mA standard differential output, which is popular for noisy environments, across long distances using twisted-pair wires to a 4- to 20-mA differential receiver, such as TI's RCV420. Versatile linearization circuitry provides a second-order correction to the RTD, typically achieving a 40-fold improvement in linearity (**Figure 2**).

Thermocouples are rugged, have a temperature range of −184 to +2300°C, and are inexpensive. On the downside, they are highly nonlinear and typically need significant linearization algorithms. Their voltage output is also relatively low, so they require analog amplifier-gain stages and cold-junction compensation (**Figure 3**).

Rather than measure absolute temperature, thermocouples measure the temperature difference between two points. To measure a single temperature, thermocouples maintain one of the junctions—normally the cold junction—at a known reference temperature and the other junction at the temperature they want to sense. Although having a junction of known temperature is useful for laboratory calibration, it is inconvenient for most measurement-and-control applications. Thermocouples instead incorporate artificial cold junctions using thermally sensitive devices, such as thermistors or diodes, to measure the temperature of the input connections at the instrument. Special care must be taken to minimize any temperature gradient between terminals. Hence, you can simulate the voltage from a known cold junction and apply the appropriate correction.

Thermistors, whose temperatures range from 0 to 100°C, are inexpensive and come in small packages; however, they require temperature compensation in the form of a look-up table and also need an excitation current, as do RTDs. Thermistors have either an NTC (negative temperature coefficient) or a PTC (positive temperature coefficient). Most PTC thermistors are switching devices, meaning that their resistance rises suddenly at certain critical temperatures. For this reason, you can use them as current-limiting devices for circuit protection. You can use NTC thermistors for temperature measurement as resistance thermometers, but calibration is necessary if the application operates over large changes in temperature. For applications operating over small changes in temperature, the resistance of the material is linearly proportional to the temperature—if you select the appropriate semiconductor (**Reference 1** and **Figure 4**). You can also use thermistors in a bridge configuration in the same way that you do to solve lead resistance in RTDs and feed the differential output into an amplifier.

The most common active temperature sensors, digital temperature sensors, yield high accuracy from the sensor to the microcontroller. Their data sheets specify both drift and repeatability; they need no calibration, and they are highly integrated. Examples of these devices include On Semiconductor's ADT7484A and Texas Instruments' TMP006, an example of miniaturization, integration, and innovation. This device is the first in a series that measures the temperature of an object without making contact with the object. The high level of integration allows the output to include a digital serial SMBus (system-management bus) and a chip-

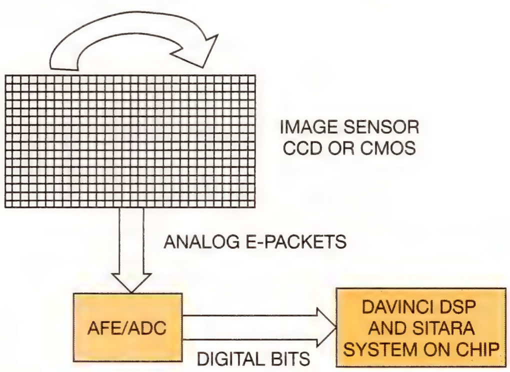


Figure 5 Texas Instruments' VSP2582 analog front end conditions and digitizes the sensor output and sends the data to a DSP.

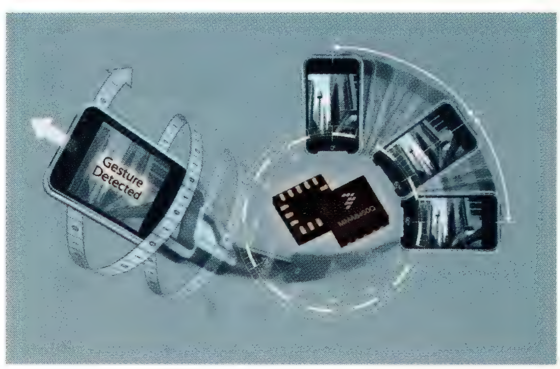


Figure 6 Freescale's tiny, low-power, handheld MMA8450Q motion sensor has an onboard DSP for motion applications.

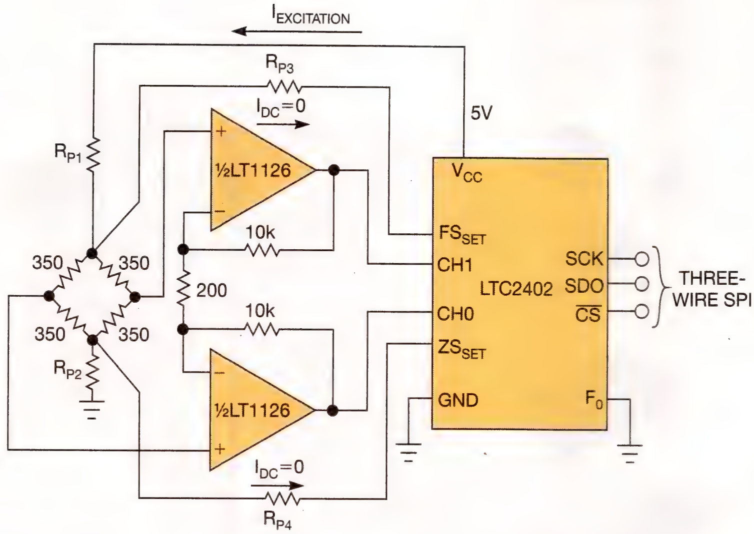


Figure 7 A discrete bridge pressure sensor needs a constant current excitation, which greatly improves the temperature dependence of the bridge over the voltage-source drive, and a differential-amplifier input conditioner for amplification and common-mode noise rejection (courtesy Linear Technology).

scale package. Atmel's temperature-sensor portfolio also includes a variety of options.

Image sensors typically use analog CCD (charge-coupled device) or CMOS technology. A CCD converts light in the form of photons into an electrical signal in the form of electrons and requires CDS (correlated double sampling) to condition the sensor. An active-pixel CMOS imaging chip uses a CMOS-semiconductor process and requires a sample-and-hold device. Extra circuitry next to each photo sensor converts the light energy to a voltage. The chip may include additional circuitry to convert the voltage to digital data.

FOR MORE INFORMATION

Analog Devices
www.analog.com

Bosch-Sensortec
www.boschsensortec.com

Freescale
www.freescale.com

Intersil
www.intersil.com

Linear Technology
www.linear.com

Maxim Integrated Products
www.maxim-ic.com

Measurement Specialties
www.meas-spec.com

National Semiconductor
www.national.com

NXP
www.nxp.com

On Semiconductor
www.onsemi.com

STMicroelectronics
www.st.com

Texas Advanced Optoelectronic Solutions
www.taosinc.com

Texas Instruments
www.ti.com

Interfacing and signal conditioning can involve processes as simple as an integrated, high-speed ADC, such as NXP's TDA8784, or an AFE (analog front end), such as Texas Instruments' VSP2582 (**Figure 5**). The AFE or the ADC conditions and digitizes the sensor output and sends the data off to a DSP.

Display management is a critical part of any consumer product, especially battery-dependent devices. Intersil offers a great selection of light-to-digital and light-to-analog sensors for backlight control and ambient-light sensing for mobile or fixed devices with a display. Intelligent optoelectronic sensors from TAOS (Texas Advanced Optoelectronic Solutions) simplify the measurement and analog-to-digital conversion of light and reduce the need for signal-conditioning or preprocessing circuitry in light-centric systems.

Many position and motion sensors are available, including Freescale's low-g-force-acceleration sensors, which detect orientation, shake, tap, double tap, fall, tilt, motion, positioning, shock, or vibration. The company's handheld MMA8450Q has an integrated DSP (**Figure 6**). You can configure this intelligent, low-power, low-noise accelerometer to generate inertial wake-up-interrupt signals when a programmable acceleration threshold is crossed on any of three sensed axes. End users can program the acceleration and time thresholds of the interrupt generators. Other tiny, low-power sensors in the industry have easy serial interfaces to DSPs for motion applications.

MEMS piezoresistive bridge sensors are the most common devices for measuring pressure. Bosch-Sensortec features a variety of such sensors in its product portfolio. Designers can also use bridge pressure sensors in discrete designs with analog conditioning circuitry for custom applications. Measurement Specialties, for example, offers the MS7301-D series of bridge piezoresistive devices in die form. A discrete bridge pressure sensor needs a constant current excitation, which greatly improves the temperature dependence of the bridge over the voltage-source drive, and a differential-amplifier input conditioner for amplification and common-mode-noise rejection can be used because bridge sensors typically output 2 mV/V full-scale (**Figure 7**). You can also use an instrumentation amplifier, which has high input impedance, for high-impedance bridges. A 24-bit sigma-delta ADC has a high dynamic range for better resolution (**Reference 2**). Good design architectures to signal-condition these sensors couple with DSPs or microcontrollers to provide improved safety and security in vehicles, smarter performance in ubiquitous home networks, location data from a gamut of possible inputs, and more realistic experiences in gaming electronics.EDN

REFERENCES

1 "A Simple Thermistor Interface to an ADC," Maxim Integrated Products, Application Note 1753, Nov 26, 2002, http://bit.ly/qP668I.

2 Mayes, Michael K, and Derek Redmayne, "1- and 2-Channel, No Latency ΔΣ, 24-Bit ADCs Easily Digitize a Variety of Sensors," *Linear Technology Magazine*, Volume 10, No. 1, February 2000, pg 1, http://bit.ly/q2TILV.


New AV Series
Isolated
100 to 5000 VDC Output
Surface Mount/Thur-Hole
New Dual Isolated Outputs
to 250 VDC Isolated Output
Thru-Hole and Surface Mount
VV Series
Up to 10,000 VDC Output
Up to 10 Watts
A/SM Series
Surface Mount/Thur-Hole
Isolated
3.3 to 1000 VDC Output
AVR Series
Regulated to IKV
Low Noise
M/MV Series
Military Components
Military Environmental
Testing Available
3.3 to 500 VDC
HVP Series
Programmable to
6000 VDC Output
LV/HV Series
36 to 170 Inputs
Terminal Strips
PC Board Mount
3.3 to 48 VDC Output
OR/IR/JR/KR Series
Wide Input Range
8 to 60 VDC
2 to 100 VDC Output
Regulated
DC-DC Converters
2V to 10,000 VDC Output
2500 Standard Models
Regulated/isolated
Wide Input Available
1 Watt to 300 Watts
P/HP/XP Series
HIGH POWER
3.3 to 350 VDC
Output
Isolated to
300 Watts
LF/LM/FM Series
-40° and -55° to +85°C
Operating Temperature
3.3 to 350 VDC outputs
in 1/2 Brick and Full Brick
• COTS
• MILITARY
• INDUSTRIAL
LP Series
Wide Input Range
Watts to 75 Watts
2 to 100 VDC Output Full Brick
PICO
Also AC-DC single and/or 3 Phase. Power Factor Corrected. 3 Watts to 2000 Watts Models.
Electronics, Inc. 143 Sparks Ave. Pelham, NY 10803
• Call Toll Free 800-431-1064 • Fax: 914-738-8225
ISO CERTIFIED 9001:2000
SURFACE MOUNT • MILITARY UPGRADES • 2500 Standard Models • Custom Models
www.picoelectronics.com
E-mail: info@picoelectronics.com • Send for free 180 pg PICO Catalog

BY ASHISH GOEL AND ATEET MISHRA • FREESCALE

Latches and timing closure: a mixed bag

LATCHES HAVE THE EDGE OVER FLIP-FLOPS IN HIGH-FREQUENCY DESIGN. HERE ARE SOME HINTS ON APPLYING THEM TO YOUR NEXT DESIGN.

Digital blocks contain combinational and sequential circuits. Sequential circuits are the storage cells with outputs that reflect the past sequence of their input values, whereas the output of the combinational circuits depends only on the current input. Latches and flip-flops are common storage elements for these blocks.

A latch is a level-sensitive storage cell that is transparent to signals passing from the D input to the Q output and that holds the values of D on Q when the enable signal is false. Depending on the polarity of the enable input, latches have either a positive level or a negative level. A flip-flop, on the other hand, is an edge-triggered device that changes state on the rising or the falling edge of an enable signal, such as a clock. In a rising-edge-triggered flip-flop, the flip-flop samples its input state only at the rising edge of the clock. It then maintains this sampled value until the next rising edge of the clock. Designers typically prefer flip-flops over latches because of this edge-triggered property, which simplifies the behavior of the timing and eases design interpretation.

Latch-based designs, however, have smaller dice and are more successful in high-speed designs in which the clock frequency is in the gigahertz. In flip-flop-based high-speed designs, maintaining clock skew is a problem, but latches ease this problem. Hence, the use of flip-flops can limit the design's performance when the slowest path limits the frequency of the design. When you consider process variation, latch-based design is dramatically more tolerant of variations than is flip-flop-based design, resulting in better yield, allowing more aggressive clocking than the equivalent design with flip-flops, or providing both of these benefits.

USING LATCHES TO BORROW TIME

Latches' biggest advantage is that they allow a sufficiently long combinational path, which determines the maximum frequency of the design, to borrow some time from a shorter path in subsequent latch-to-latch stages to meet its timing goal. A level-sensitive latch is transparent during an active clock pulse. The time-borrowing technique can also relax the normal edge-to-edge timing requirements of synchronous designs (**Figure 1**).

A sample circuit has two timing paths (**Figure 2**). Path 1 goes from a positive-triggered register (1) to a negative-level latch (2). Path 2 goes from the latch to a positive-edge-triggered register (3). In the **figure**, borrowing compensates for the delay through the logic cloud (A). The logic in Path 1 incurs a delay, and, depending on the length of that delay, two possible scenarios of timing analysis can emerge. These scenarios decide how much time the design can borrow (**figures 3** and **4**).

In **Figure 3**, data arrives from Logic A at Latch 2 before the falling edge of the clock at the latch. In this case, the behavior of the latch is similar to that of a flip-flop, and the analysis is simple. You need not borrow any time to achieve your timing goal. In **Figure 4**, the negative clock edge enables the latch before the arrival of the signal from Logic A at the input of the latch, so the latch enters transparent mode and for a time transmits an undefined state from Logic A through to Register B. It is important that the new state from Logic A reaches and passes through Logic B in time to meet the setup requirements of Register 2. So, if Logic B has a short propagation delay, you can, in effect, let Logic A have some of the time you reserved

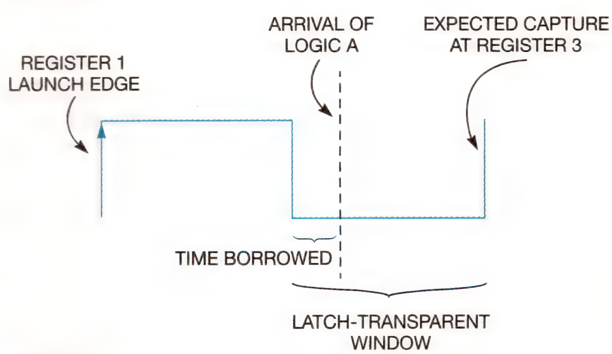


Figure 1 The time-borrowing technique can relax the normal edge-to-edge timing requirements of synchronous designs.

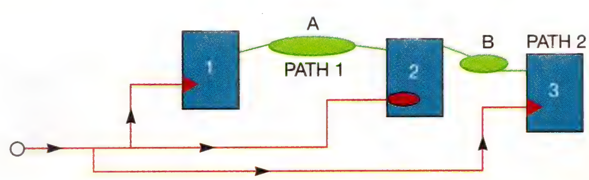


Figure 2 Path 1 goes from a positive-triggered register (1) to a negative-level latch (2). Path 2 goes from the latch to a positive-edge-triggered register (3).

for Logic B, and the circuit will still work. Logic A borrows this extra time to complete its propagation delay. When Path 2 is timed, the timing analysis considers the end of the borrowed time as the starting point for analyzing Logic B's delay.

Static-timing analysis generates timing reports according to the examples shown in **figures 3** and **4**. However, the timing when the latch is enabled is the same as if the latch were simply a transparent delay element (**Figure 5**).

TIME-BORROWING IN OCV

In an ideal scenario, the time at the starting point should equal the time the latch borrows. Due to shrinking process technology, however, OCV (on-chip variation), signal-integrity, and other factors come into play. To increase the accuracy of the analysis, you can also use CPPR (common-path-pessimism-removal) techniques. These factors complicate the relationship between time-borrowing and time for the starting point. As a result, the timing analysis of latches becomes more challenging.

Returning to **Figure 4**, you'll note an interesting relationship between time-borrowing and the starting-point time. The variables include clock uncertainties, clock-path pessimism due to OCV, and clock derating. During the timing of Path C, $T_{SP}=T_B-U+CPPR$, where T_{SP} is the time for the starting point and T_B is the time Path 1 borrows when constraining Logic A.

Applied uncertainty in Path 1 is the uncertainty for the clock path of the latch, which is not part of pessimism when the latch is transparent. You thus remove that pessimism about the latch clock's uncertainty from the start time. Similarly, you recover pessimism due to CPPR in the time for the starting point because the same early or late path type of latch-launch clock path is in Path 2. If you want to apply clock derating in the design during the timing of Path 2, you should consider using early rather than late derating to make the path the same as the capture clock of Path 2.

EDA tools usually exhibit pessimistic behavior when timing Path 2 because they don't consider CPPR, but they should not apply that pessimism. Path 1's clock-path pessimism ends during calculation of the start-point time, and again, you should not retain this pessimism. The latch is transparent, so it acts as a combinational cell. In this case, you should consider using CPPR between the starting point of Path 1 and the ending point of Path 2. These tools yield extremely pessimistic results because they fail to consider that the use of pessimism is acceptable.

You can also consider using the smallest value between the CPPR of Path 1 and that of Path 2. This approach is not the most accurate, but it provides another level of pessimism removal. Comparing the common clock path of the register and the latch in timing Path 1 versus the common clock path of the latch and the endpoint—the second register—in timing Path 2 can give an idea of the minimum possibility of the clock path between the register and the final endpoint.

Once you ensure that the latch will be transparent during path timing, the least preferred, most accurate, and best way to judge the timing of latches is to make the latch transparent by using a case analysis on the enable pin of the latch. After this step, the EDA tool can time the two segments as one complete path. This method is the least preferred because the latch may not always be transparent when timing Path 1 in the best-case condition: when time borrowing is unnecessary.

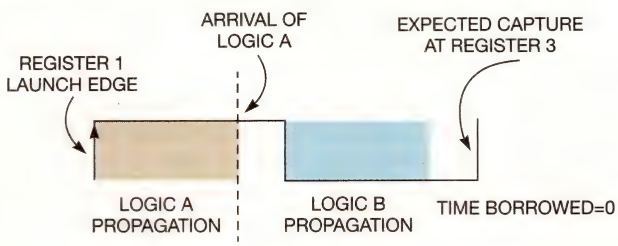


Figure 3 When Logic A is fast enough, no borrowing is necessary.

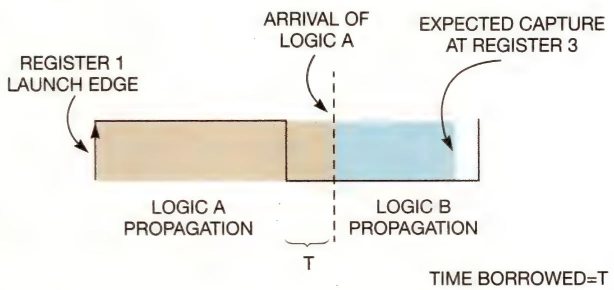


Figure 4 Logic A borrows time from Logic B.

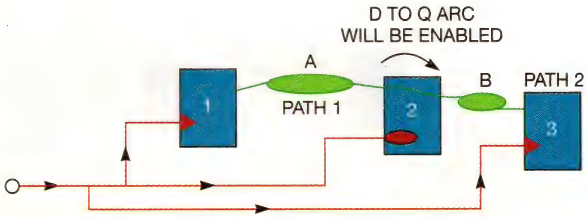


Figure 5 When the latch is enabled, it essentially becomes a passive delay.

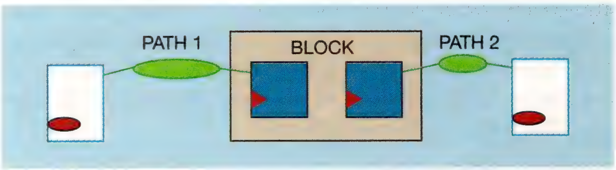


Figure 6 A block interfaces to external latches.

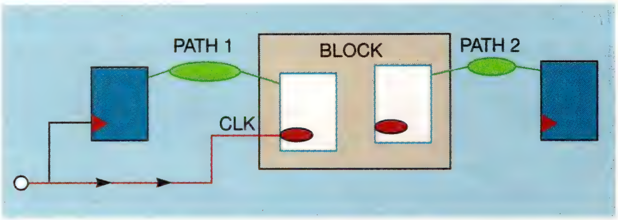


Figure 7 A block using latches interfaces to external registers.

The tool also misses all the paths that do not require time borrowing and holds a time check at the latch's endpoint.

PARTITIONING CHALLENGES

Some challenges occur in hierarchical design when the blocks have latch-based interfaces. The timing tools require help to understand when it is possible to borrow time across a block boundary. The first challenge is to enable time-borrowing for the ports that you have budgeted for timing. When timing a block, you can model the ports that are entering or exiting latches at the top level of the SOC (system on chip) by using their proper I/O delays and the level-sensitive option in the EDA tool. Consider the case for Path 2 (**Figure 6**). Without the level-sensitive option, this path could be critical at the block level. By defining the output delay at the output port with the level-sensitive option, the timing tool can borrow time from the input stage of the next block, and this ability relaxes the timing on the output port.

Next, consider a case in which the latches are inside rather than outside the block (**Figure 7**). Path 1 has no special requirements for closing the block, but you must define all types of clock latency—rise, fall, minimum, and maximum times—for the CLK pin. This approach helps you correctly calculate the time of the starting point employing OCV and CPPR. In this way, you'll get no surprises when you merge the block at the top level. Another challenge arises when you use the timing models for top-level execution. You can enable time-borrowing through boundary latches by using gray-box ETMs (extracted timing models), which preserve the boundary latch and generate ETM libraries.

In summary, latches are beneficial for high-speed-SOC designs, but their use adds challenges in static-timing analysis, especially with hierarchical design. The limitations of EDA tools increase the complexities of latch-based design. You can employ latches in SOCs only after careful analysis. You can then apply some of these techniques, which can reduce the complexities of designing with latches. **EDN**

ACKNOWLEDGMENT

This article originally appeared on EDN's *sister site, EDA Designline (http://bit.ly/p3aN3C).*

AUTHORS' BIOGRAPHIES

Ashish Goel is a lead design engineer at Freescale in India. He has 11 years of industry experience in static-timing analysis, RTL (register-transfer-level) design, physical design, and formal technologies. Previously, he worked at STMicroelectronics, Agilent Technologies, and Infineon Technologies. Goel holds multiple patents in FPGA architecture.

Ateet Mishra is a senior design engineer at Freescale in India, where he has worked for six years. He has experience in static-timing analysis, physical design, and synthesis. He has successfully taped out multiple SOCs.

Eight LEDs make a 100-division voltmeter

Raju Baddi, Tata Institute of Fundamental Research, Pune University, Maharashtra, India

DIs Inside

▶To see all of *EDN*'s Design Ideas, visit www.edn.com/designideas.

The circuit in this Design Idea makes a voltmeter that reads to 0.99V. The idea uses a counter IC to drive two sets of four LEDs (**Figure 1**). Each of these two sets represents a BCD (binary-coded-decimal) value. With all of the LEDs off, the voltmeter reads 0V. With all of the LEDs on, the reading is 0.99V. Op amp IC_{1A} generates a predictable voltage ramp.

You use op amp IC_{1B} as a comparator to compare the ramp to an input signal. The higher the input voltage, the longer the output pulse from IC_{1B} is. You use this pulse to gate free-running oscillator IC_{2B}. A potentiometer on this multivibrator circuit allows you to adjust the full-range count. The voltmeter has a maximum input of 1V and uses three dual-part packages. You make output counter IC_3 work as a two-digit counter by strapping the enable pin of the IC_{3B} part to the MSB (most-significant-bit) output of the IC_{3A} part.

A dual op amp is used to create the comparator function and the ramp generator. The design also uses a dual 555-type timer chip. You use IC_{2A} to

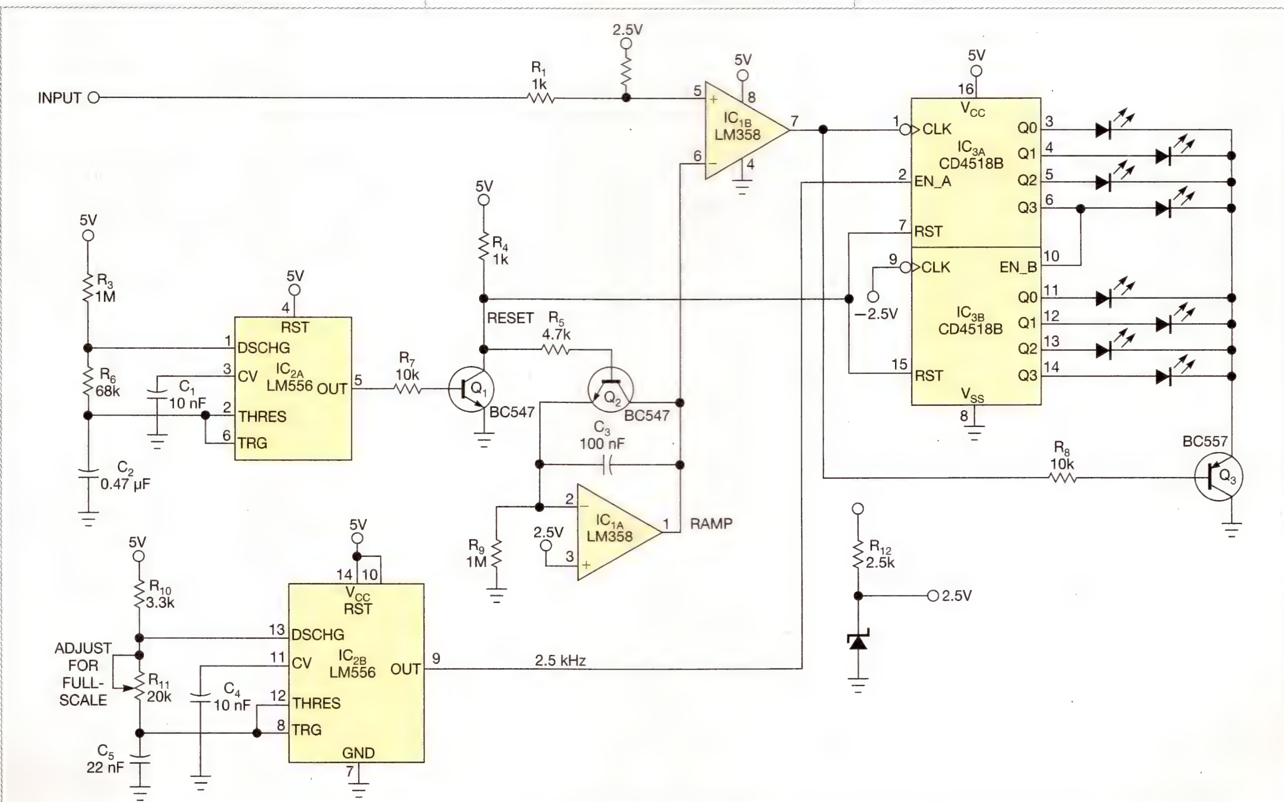


Figure 1 This 100-division voltmeter uses three simple chips.

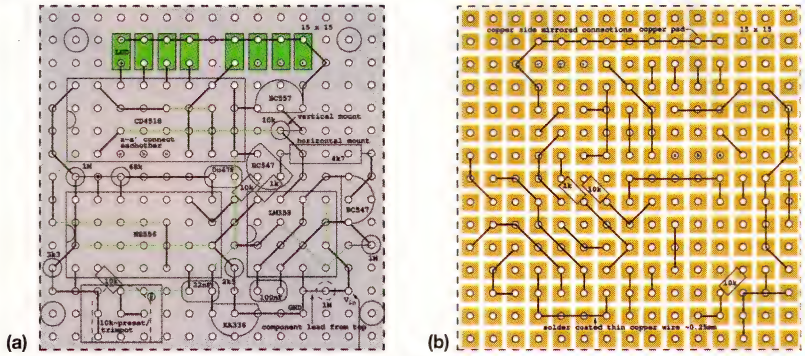


Figure 2 A top view of a 15×15-hole prototype board shows component placement and connections on the top (green) and bottom (black) for the voltmeter circuit (a). A bottom view of the board shows the connection on the bottom, along with three resistors (b). For a full-size view of this figure, go to www.edn.com/110922dia.

create the ramp and to reset it and the output counter, and you use IC_{2B} as a free-running oscillator that drives the counter chip. To blank the output LEDs when the chip is counting, Q_3 disables drive current to the LEDs when IC_3 is incrementing. You use IC_4 to derive a reference of 2.5V.

Tests of the design use TL084 op amps, but you can also use an LM358. A top view of the 15×15-hole prototype board shows component placement (**Figure 2a**). **Figure 2b** shows a bottom view of the board, with the connection and three resistors. You might use flat-green LEDs with the sides painted black or covered with black-plastic sleeves for good visibility. EDN

Simple circuit controls the rate of voltage change across a capacitor or another load

Fabien Dubois, Ampere Lab, Lyon, France

The circuit in this Design Idea lets you set a well-controlled voltage rate of change, often expressed as the differential dV/dt (instantaneous rate of voltage change over time in volts per second). You can vary the sensitivity with a potentiometer. Set the dV/dt from 1V/200 nsec to 1V/3 msec. The input voltage can range from a few volts to 30V. Higher-voltage transistors can be used to increase the upper voltage limit. The circuit precharges a capacitor with a slow and controllable dV/dt to avoid a large inrush current during power-up. You can also use the circuit to create a high dV/dt for susceptibility testing on other circuits.

The circuit uses a P-channel MOSFET, Q_1, to control the rate of change of the output voltage (**Figure 1**). You drive the MOSFET with a constant-current source comprising Q_4 and R_{CS}, which feeds gate-to-source resistor R_{GS}. Applying a positive control voltage to the base of Q_4 draws a current that creates a voltage across R_{GS}. This voltage occurs across the gate and source of Q_1, turning it on. The circuit uses capacitor C_{DVS} as a sensing device of the rate of change of the output voltage. Voltage variations across C_{DVS} generate a current that creates a current proportional to the dV/dt, as the following **equation** shows:

$$I_{CS}=C_{DVS}\times\frac{dV_{OUT}(t)}{dt}.$$

Resistor R_{DVS} converts this current into a voltage signal. When that voltage reaches approximately 0.67V, it turns on Q_2, which turns on Q_3. The current that Q_3 supplies from the input tends to lower the Q_1 gate-to-source voltage and reduces its drive. You use R_B to limit the base current of Q_2. This servo action puts the gate-to-source voltage of the MOSFET in the Miller plateau, a constant-current region of the FET's characteristic curve. The FET has an internal Miller capacitance, C_{GD}, between the gate and the drain pins.

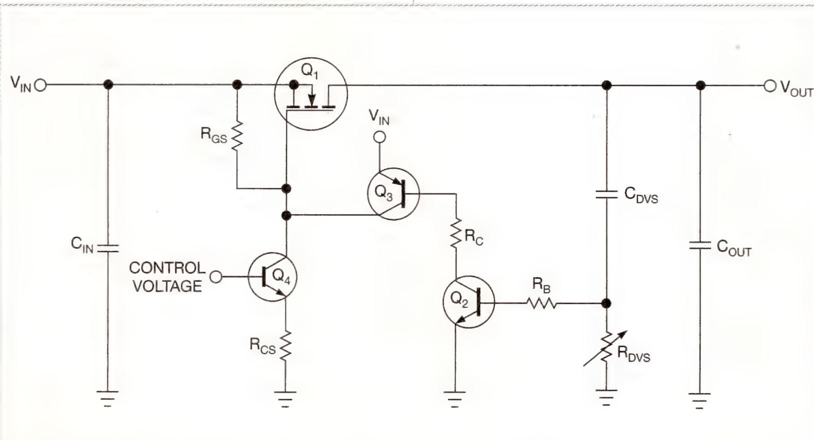


Figure 1 This circuit creates a fixed dV/dt based on the control voltage and the setting of R_{DVS}.

TABLE 1 CIRCUIT PART NUMBERS

Component	Description	Manufacturer	Part no.
C_{IN}	10-µF, 50V tantalum capacitor	AVX	TPSE106K050R0500
C_{OUT}	1-µF, 50V ceramic capacitor	AVX	12065C105KAT2A
C_{DVS}	10-nF, 50V ceramic capacitor	AVX	08055C103KAT2A
Q_2 and Q_4	40V, 0.6A NPN transistor	On Semiconductor	MMBT2222ALT1G
Q_3	60V, 1.2A PNP transistor	On Semiconductor	MMBT2907ALT1G
Q_1	100V, 4A power MOSFET	Vishay	IRF9510SPBF
R_B	1-kΩ, 0603, 1% resistor	Vishay	CRCW12061K00FKEA
R_C	1-kΩ, 0603, 1% resistor	Vishay	CRCW12061K00FKEA
R_{CS}	10-kΩ, 0603, 1% resistor	Vishay	CRCW120610K0FKEA
R_{DVS}	10-kΩ trimming potentiometer	Bourns	3362W-1-503LF
R_{GS}	10-kΩ, 0603, 1% resistor	Vishay	CRCW120610K0FKEA

The circuit's constant-current source controls the charge current of this Miller capacitance. As transistor Q_3 injects current to the gate, Miller current I_{GD} decreases and the slope of the output voltage decreases accordingly, as the following **equation** shows:

$$\frac{dV_{dS}(t)}{dt}=\frac{I_{GD}}{C_{GD}}.$$

The feedback loop keeps the dV/dt ratio constant. The rate of change of the output voltage is a function of the base-emitter voltage of Q_2, R_{DVS}, and C_{DVS}, as the following **equation** shows:

$$\frac{dV_{OUT}(t)}{dt}\simeq\frac{V_{BEQ1}}{R_{VDS}\times C_{DVS}}.$$

You can build the circuit with the part numbers in **Table 1**. EDN

LED bar-graph display represents two digits

Ajoy Raman, Bangalore, India

This circuit uses two National Semiconductor (www.national.com) LM3914 dot/bar-display-driver ICs to implement a two-digit, 0 to 5V LED voltmeter that mimics a subranging flash ADC. An LED bar graph comprising five LEDs, each representing 1V of input signal, represents the MSD (most-significant digit). Nine LEDs in dot mode, in which only one LED lights, represent the LSD (least-significant digit). The circuit senses the operation of the MSD LEDs and uses them to change the input reference ladder of the chip that drives the LSD. The input signal ranges from 0 to 5V, and accuracy is better than ±50 mV. The circuit operates over a supply voltage range of 5 to 8V.

R_1 and R_2 divide the input voltage in half, such that a 5V maximum input is 2.5V at the LM3914s, IC_1 and IC_2 (**Figure 1**). You strap the mode pin of IC_1 high, so it operates as a bar graph, and use V_{R1} to adjust the REFOUT pin of IC_1 to 2.5V. Thus, each of the IC_1 output pins lights successively in 0.5V increments. Because this IC makes the MSD, you wire in only five LEDs on every other output, starting at output D_2, meaning that the five LEDs will light at 1V intervals from 1 to 5V. The LM3914's data sheet explains how you can use R_3 to set a constant-current output on the LED pins (**Reference 1**). The current in each LED is approximately 10 times the current that you draw from the REFOUT output pin. The part maintains 1.25V between the REFADJ and REFOUT pins. The $V_{R2}/R_{10}/R_{13}$ voltage divider causes a load, which, along with the 1.5-kΩ value of R_3, sets a fixed output current in LEDs D_1 through D_5. You should select these LEDs from the same batch so that their forward voltage drops match.

You then wire a resistor and a transistor around each of the four LEDs. The voltage across the LED also presses across the resistors, so these LEDs form four constant-current sources that operate in conjunction with the LEDs. Adjust V_{R3} such that each LED when on

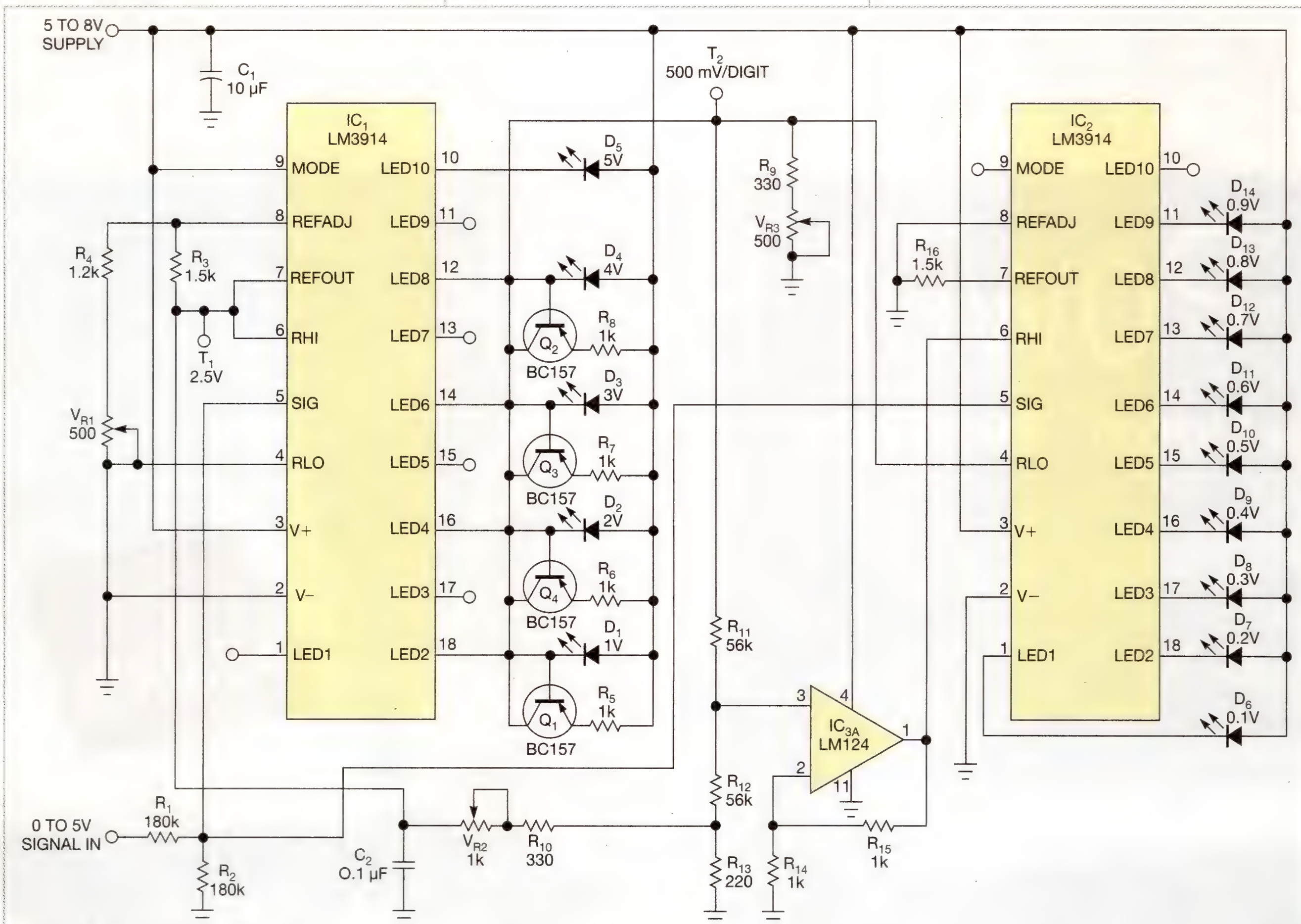


Figure 1 This voltmeter displays 1 to 5V as a bar graph from IC_1. A dot display from IC_2 represents the least-significant digit, with the LEDs representing 0.1 to 0.9V.

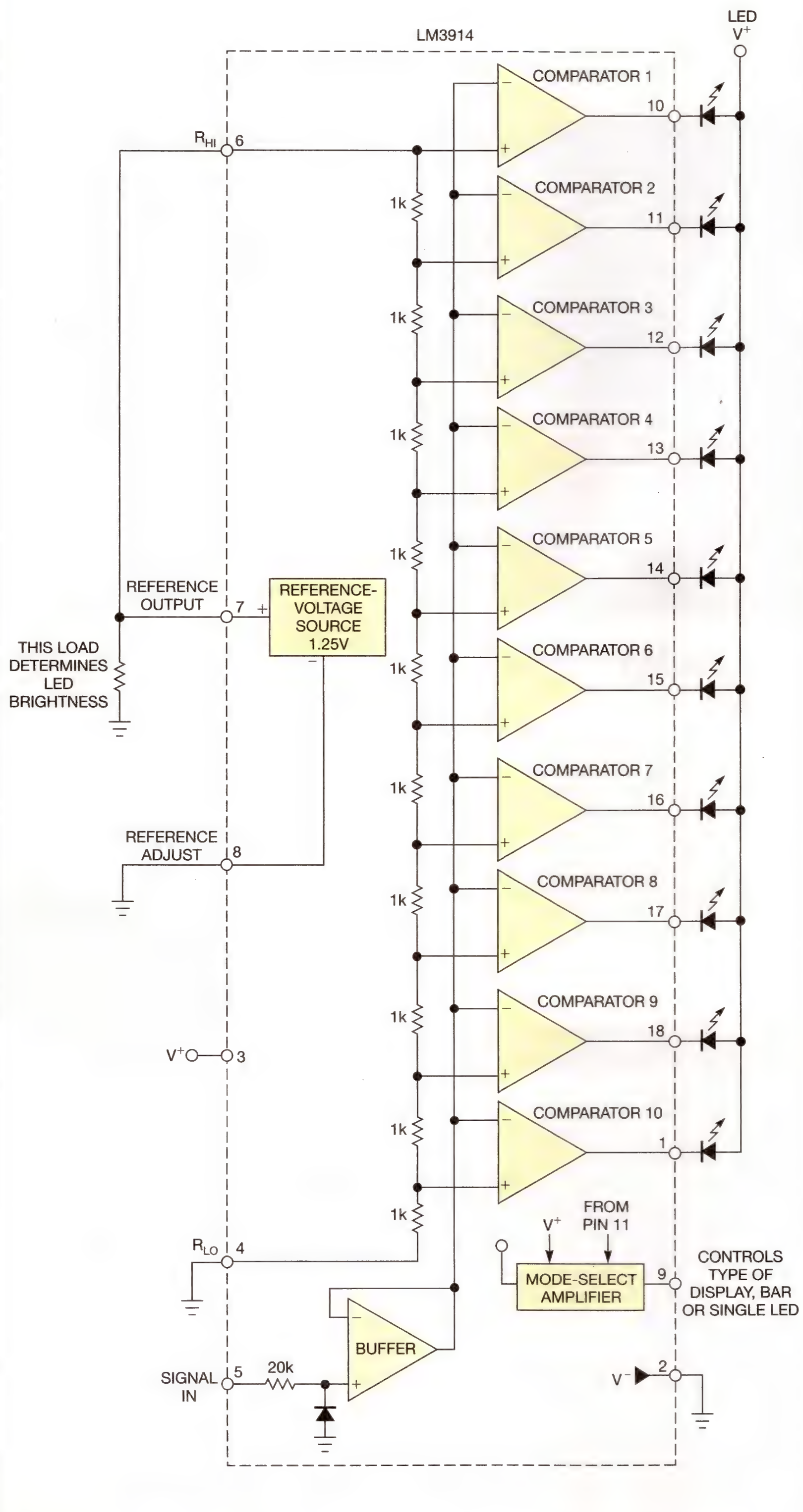


Figure 2 The LM3914 IC has an internal reference and a resistor ladder you can configure to make bar or dot LED displays (courtesy National Semiconductor).

adds 500 mV to their summed output. You send this signal to R_{LO}, the bottom of the internal resistor string in the second LM3914 (**Figure 2**). You then send the 50%-divided input signal to the SIG Pin of IC_2. Use an op amp, IC_3, to add a fixed 500-mV offset plus the summed-current signal from the outputs of IC_1. R_1 and R_2 reduce the input signal to the circuit by 50%, so a 500-mV excursion at IC_2's SIG Pin input represents 1V of the input excursion.

LEAVE THE MODE PIN ON IC_2 FLOATING SO THAT THE PART OPERATES IN DOT MODE, NOT BAR MODE.

As the input to the circuit goes from 0 to 1V, the SIG inputs to both bar-graph ICs go from 0 to 0.5V. No LEDs light on IC_1, meaning that IC_2 has R_{LO} at 0V and R_{HI} at the 500-mV offset you adjusted with V_{R2}. The LED outputs of IC_2 now light in sequence as the input to the chip goes from 0 to 0.45V, corresponding to a 0 to 0.9V input at the Signal-in Port. When the input signal is high enough to light LED D_1, the value at IC_2's R_{LO} jumps to 500 mV, and the input at R_{HI} jumps to just 500 mV higher than R_{LO}, or 1V. Because IC_2's internal resistor ladder is now biased between 0.5 and 1V, IC_2 indicates 0.1V steps between 1 and 2V at the Signal-in Port. Leave the Mode Pin on IC_2 floating so that the part operates in dot mode instead of bar-graph mode.

At a 4.9V input to the Signal-in Port, LEDs D_1 through D_4 illuminate, resulting in 2V at the R_{LO} input of IC_2. The op amp adds 500 mV to that value and presents it to the R_{HI} input of IC_2 for a total of 2.5V. The input to IC_2 is 2.45V, so the D_9 output of IC_2 lights D_{14}, correctly indicating the LSB (least-significant bit) of the measurement as nine-tenths. EDN

REFERENCE

1 "LM3914 Dot/Bar Display Driver," National Semiconductor, February 2003, http://bit.ly/naDCRG.

productroundup

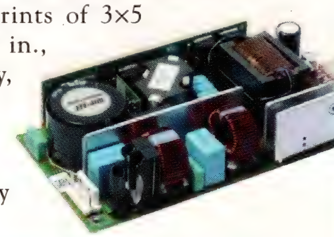
POWER SOURCES

Automotive-LED driver from Supertex reduces board space, improves reliability

The AT9919 LED-lamp-driver IC targets use in solid-state-lighting automotive applications, including headlights, taillights, brake-indicator lights, dome lights, and panel backlights. The AEC-Q100-compliant device drives LEDs using a buck topology. It comes in a compact, eight-lead DFN package. A PWM-control signal achieves LED brightness, an=d the IC drives loads of as much as 1A at more than 90% efficiency at input voltages of 4.5 to 40V. Price for the AT9919K7-G is 98 cents (1000).
Supertex Inc, www.supertex.com

TDK's digital 300 to 400W supplies meet medical and ITE safety specs

The vendor has extended the warranty of its EFE300-400M series of digitally controlled 300 to 400W power supplies from three to five years, based on the product's conservative design and field-reliability data since its introduction in 2008. Targeting use in medical and ITE (information-technology-equipment) applications, the devices have a 4-kV-ac reinforced input-to-output isolation of 1500V ac and meet the rigorous international-safety standards of IEC/UL 60601-1 for medical equipment, making them suitable for use in body and body-floating-type medical and dental applications. Regulated dc outputs of 12, 24, or 48V dc are standard, and other voltages are available. The 300 and 400W devices have footprints of 3×5 or 3.5×6.5 in., respectively, and 1.34- to 1.6-in., less-than-1U profiles. They



EDN ADVERTISER INDEX

provide 400W continuous power and as much as 475W peak power for 10 sec. The supplies include a magnetic transformer, with the transformer and the inductor windings on the same core, to boost efficiency to typically 90%, and they employ an 8-bit microcontroller for full digital control of the output and to handle housekeeping routines. Prices start at $164.42 (100).
TDK-Lambda Americas,
www.us.tdk-lambda.com/lp/products/efe-series.htm

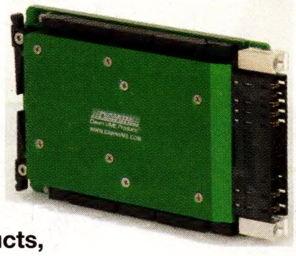
Power Partners' 150W PPWAD150 desktop power supply features active PFC and Level 5 efficiency

The PPWAD150 series of power supplies has active PFC and provides 150W of desktop power in a

6.69×3.35×1.73-in. package. With no-load standby power of 0.5W or less and average efficiency of 85% or better, the PPWAD150 series complies with Energy Star Efficiency Level V requirements and complies with ROHS directives. The series has a 90 to 264V-ac input and offers six single-output models ranging from 12 to 48V dc. Operating temperature is 0 to 40°C; the devices require no minimum load and maintain a 5/–2% tolerance through the full load range. Prices start at $51 (OEM quantities).
Power Partners Inc,
www.powerpartners-inc.com

Dawn's 3U PSC-6234 VPX power supply complies with VITA 62

The VITA 62-compliant, 3U PSC-6234 power supply features a VITA 62 power-connector pinout and full OpenVPX support. The device suits use in mission-critical applications that operate over a wide range of temperatures at high power levels. The unit's six-channel design provides as much as 400W output at a 28 or 48V input on a 1-in. pitch. Input voltage ranges from 18 to 36 and 36 to 75V dc. The PSC-6234 has 12, 3.3, and 5V voltage rails; auxiliary voltages of 12, –12, and 3.3V; and typical battery voltage of 3V. The device sells for $3890 (one).

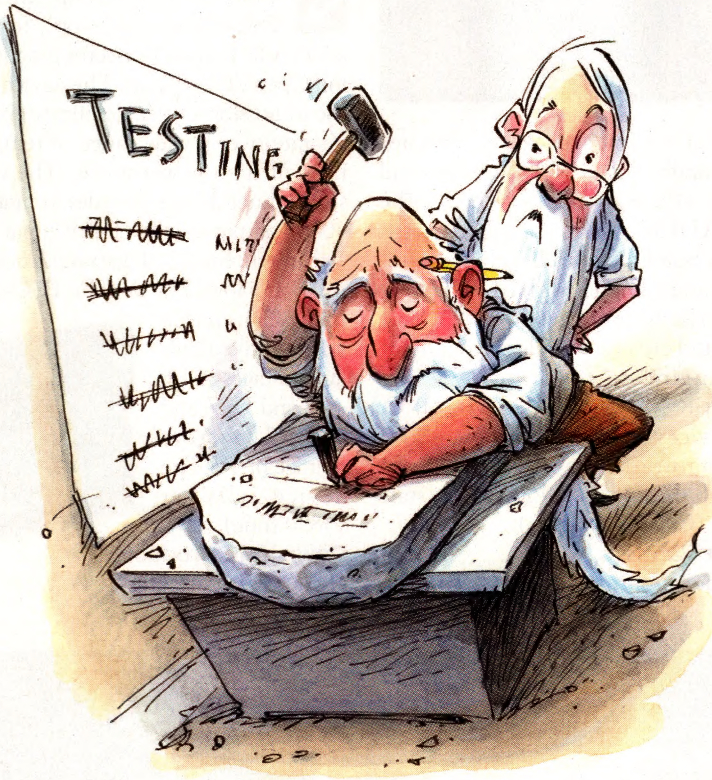


Dawn VME Products,
www.dawnvme.com

EDN productmart

This advertising is for new and current products.

Not set in stone



DANIEL VASCONCELLOS

In 1997, I was managing a sustaining engineering group for current storage products at a major computer manufacturer. One such product was a high-performance, high-availability, dual-redundant RAID (redundant-array-of-independent-disks)-controller system. The product used a proprietary dual-path, serial, coaxial-cable bus to interconnect the host computers and storage nodes in a storage-area network. Two years earlier, we had begun shipping this product to customers, and customers were reporting—almost from day one—a baffling problem. An internal parallel data bus was occasionally reporting parity errors on data transfers from the host port's ASIC to the shared internal buffer memory. This parallel bus was contained entirely within the PCB (printed-circuit board) and extended only a few inches. You rarely, if ever, see a parity error on a well-designed PCB, and other transfers with this memory did not generate parity errors.

This problem caused one controller of the pair to crash and reboot, thus making its attached storage unavailable to the host computers for as long as a minute during the reboot. Some customers never saw the problem, some saw it only once every few months, and several saw it often enough to complain loudly about it. The controller's error log was no help, and we were never able to force the error in our lab.

I received a call from a software-test group in a company location in another state. The group claimed that it was experiencing this failure at least weekly. I got a complete description of this group's hardware and software configuration, along with the exact test software the group was running. We reproduced a similar configuration in our lab. After a week of trial and error, our software tester was able to create the error about once a day. Now we had something to work on!

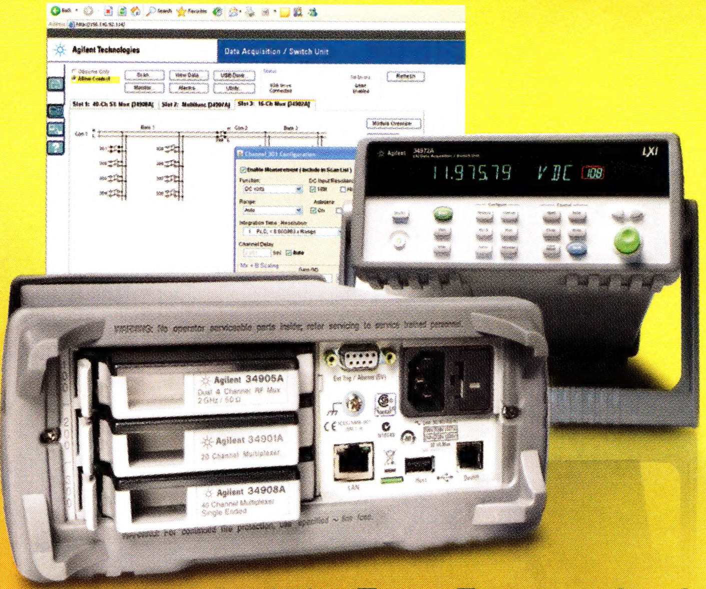
We instrumented one of the controllers in the pair with a logic analyzer. First, we verified that the parity-error flag from the internal memory controller had indeed caused the crash. Next, we looked at the internal parallel data bus when the error occurred. We discovered that, on the failing-bus cycle, all 32 data bits and four parity bits were zeros, which should never happen with odd parity.

We now had to go back to the host interface's ASIC, which had few internal logic nodes connecting to external I/O pins. The engineers who had designed the ASIC had since left the company, and the design documentation that they left behind included only schematics for part of the chip, state diagrams for the internal state machines, and a minimal functional specification.

After weeks of collecting information from many logic-analyzer traces, we concluded that three independent inputs to the ASIC had to occur within a 20- to 30-nsec window to cause an internal state machine to go to an undefined state and issue the faulty data transfer. If only two of the three inputs occurred close together or if the third input was even 1 nsec outside that window, the ASIC worked fine. Because the problem was in an ASIC in this older product, we would not be fixing it. By 1999, we released a new version, which used an FPGA to implement the host-interface function. **EDN**

Tom Fava is an independent engineering consultant in Green Valley, AZ.

Data acquisition just got a lot easier.



▶▶ Fast Forward with more ways to control and connect remotely.

The Agilent 34972A Data Acquisition Switch Unit takes our best-selling Agilent 34970A to the next level with breakthrough connectivity. For starters, you get convenient built-in LAN and USB connectivity. Plus, you can control your data acquisition remotely via Web interface. And transfer logged data to your PC with a simple flash drive. No more expensive adapters and connectors. That's easy. That's Agilent.

34972A	34970A
▶▶ USB and LAN	GPIB and RS232
Graphical web interface Benchlink data logger software SCPI programming	Benchlink data logger software SCPI programming
3-slot LXI unit with built-in 6 ½ digit DMM	
$1,845*	$1,597*

Scan the QR code or visit http://goo.gl/IsbZf to see 34972A promotion details

*Prices are in USD and are subject to change.
**Terms and conditions apply

Agilent and our Distributor Network
Right Instrument.
Right Expertise.
Delivered Right Now.

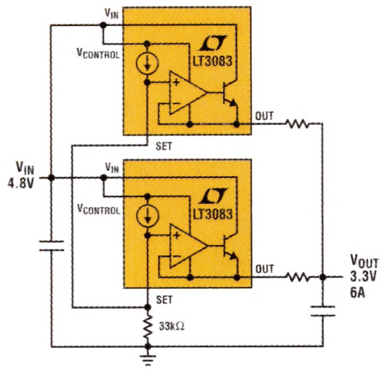
Newark element14

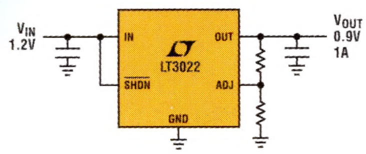
800-463-9275
www.newark.com/agilent

▶▶ **FREE 300 Mbps travel router and mobile app****
www.newark.com/Agilent_DAQ

Agilent Technologies

Not Your Dad's LDO





Selected LDOs

Product Category	Part Number	Output Current (A)	V_{IN} Range (V)	Output Voltage (V)
Current Reference-Based NPN Positive LDOs	LT®3082	0.2	1.2 to 40	Adj (0 to 38.5)
	LT3085	0.5	1.2 to 36	Adj (0 to 35.5)
	LT3080	1.1	1.2 to 36	Adj (0 to 35.5)
	LT3083	3	1.2 to 23	Adj (0 to 22.5)
Positive LDOs	LT3008	0.02	2 to 45	Adj (0.6 to 44.5), Fixed
	LT3050	0.1	2 to 45	Adj (0.6 to 44.5), Fixed
	LT3013	0.25	4 to 80	Adj (1.24 to 60)
	LT3022	1.0	0.95 to 10	Adj (0.2 to 9.5), Fixed
	LT3070	5	0.95 to 3	Adj (0.8 to 1.8)
Dual Positive LDOs	LT3029	0.5 x 2	1.9 to 20	Adj (1.215 to 19.5)
Dual Positive and Negative LDOs	LT3032	0.15 x 2	±1.9 to ±20	Adj (±1.22 to ±19.5), ±5
Negative LDOs	LT3015	1.5	–1.9 to –30	Adj (–1.22 to –29.5), Fixed

Info & Free Samples

www.linear.com/products/LDOs

1-800-4-LINEAR

Free LDO Solutions Brochure

www.linear.com/ldosolutions

LINEAR TECHNOLOGY